FIELD EFFECT TRIODES AND SPACE CHARGE LIMITED TRIODES

Report No. 3

SC Contract No. DA-36-039-sc-90756
File No. 1241-PM-62-93-93 (4941A)
DA Project No. 3A99-21-003

U.S. ARMY ELECTRONICS
Research and Development Laboratory
Fort Monmouth, New Jersey

Third Quarterly Report
1 December 1962 to 28 February 1963

Research and Development for Field Effect Triodes
and Space Charge Limited Triodes

Prepared by:

J. M. Blank
W. Tantraporn
K. K. Reinhartz
W. L. Willis
A. E. Cahill
V. A. Russell

Electronics Laboratory
General Electric Company
Syracuse, New York

FIELD EFFECT TRIODES AND SPACE CHARGE LIMITED TRIODES

Report No. 3

SC Contract No. DA-36-039-sc-90756
File No. 1241-PM-62-93-93 (4941A)
DA Project No. 3A99-21-003

U.S. ARMY ELECTRONICS
Research and Development Laboratory
Fort Monmouth, New Jersey

Third Quarterly Report
1 December 1962 to 28 February 1963

Research and Development for Field Effect Triodes
and Space Charge Limited Triodes

Prepared by:

J. M. Blank
W. Tantraporn
K. K. Reinhartz
W. L. Willis
A. E. Cahill
V. A. Russell

Electronics Laboratory
General Electric Company
Syracuse, New York

TABLE OF CONTENTS

TABLE OF CONTENTS CONT'D

LIST OF ILLUSTRATIONS

I. PURPOSE

1.1 Objectives

The purpose of this contract as outlined in the technical requirements for PR 62-ELP/R-4941 is the theoretical investigation, design, and development of thin film metal-dielectric active solid state electronic device with useable power gains that are relatively insensitive to temperature changes. The development of a multilayer structure that is capable of performing electronic amplification with performance characteristics approaching or surpassing other band gap model devices is of prime importance in this work. The development of fabrication techniques that are compatible with the production of other circuit components which lead to reproducible active devices having near optimum characteristics is also a major objective. In line with these objectives, investigations will be initiated in two major device areas; space charge limited triodes and field effect triodes.

1.2 Description of Tasks

Task I: Field Effect Triodes. This area of work is concerned with the theory and design, fabrication techniques, and electrical measurements of thin film field effect triodes. The field effect triode is a thin film active device which employs conduction of electrons from a source electrode to a drain electrode along the plane of a thin film of cadmium sulfide or other material. Modulation of the device current is obtained by a gate electrode. The gate electrode is placed on the cadmium sulfide layer between the source and drain electrodes and is insulated from the cadmium sulfide by silicon monoxide or another appropriate material.

Task II: Space Charge Limited Triodes. This area of work is concerned with the theory and design, fabrication techniques and electrical measurements on space charge limited thin film triodes. These devices consist of thin metal films which serve as emitter, grid, and plate layers. The metal layers are separated by thin films of cadmium sulfide or other appropriate materials. The grid film is deposited as a screen or grill network and is insulated from the cadmium sulfide by a material such as silicon monoxide.

Task III: Cadmium Sulfide Improvement. This section of the work is concerned with the calculation of the details of the solid gas equilibrium between cadmium sulfide, cadmium and sulfur, and the application of the results to making improved cadmium sulfide for field effect and space charge limited thin film triodes. Measurements made on these films include the determination of resistivity, Hall effect, photoconductivity, spectrum and grain size. The important characteristic quantities are the carrier density, trap depth and density, and electron mobility.

Task IV: Zinc Oxide Material Improvement. This work will be aimed at improving zinc oxide thin films and optimizing them for use in thin film field effect and space charge limited triodes. Physico-chemical reasoning as well as film fabrication and measurement approaches, similar to those described above for cadmium sulfide, will be employed in the zinc oxide material development.

1.3 Related Projects

Related Government sponsored projects include the following:

Contract Title	Contractor	Contract No.
Tunnel Cathode Investigation	General Electric Co.	DA-49-186-502-ORD-1053
Research on Thin Film Active Devices	Philco	DA-49-186-502-ORD-1056
Molecular Circuit Development	Melpar, Inc.	NOw 60-0362-C
Project Lightning	RCA	NObsr 77523
Exact Title Not Known	Electro Optical Systems, Inc.	AF 33(616)-7784
Exact Title Not Known	Philco	DA 36-039-SC-90715
Exact Title Not Known	Raytheon	AF 30(602)-2673
Exact Title Not Known	Ecole Normale	AF 61(052)-403
Exact Title Not Known	Stanford Research Institute	Nonr 225(24), NR 373360
Exact Title Not Known	MIT	NASA Res.Gr. Ns G 234-61
Exact Title Not Known	Stanford Research Institute	DA 36-039-SC-85339

(We wish to acknowledge Q.C. Kaiser, of DOFL, as the source for the last seven contracts)

II. ABSTRACT

TASK I: FIELD EFFECT TRIODES

A detailed conduction mechanism for thin-film field effect triodes is presented. New experimental findings which seem to substantiate the trap emptying mechanism are outlined. The results of experiments in varying SiO and CdS thickness in field effect triodes and their effect on device performance are shown. Effects of device aging and electrode configurations on device performance are also discussed.

TASK II: SPACE CHARGE LIMITED TRIODES

The requirements for producing space charge limited current in devices are discussed, and possible methods of fulfilling them are presented. Experimental results in fabricating devices using different source and drain electrode materials are shown. A change to the field effect triode configuration is proposed.

TASK III: CADMIUM SULFIDE IMPROVEMENT

A post-deposition treatment of cadmium sulfide films is outlined and results are presented. Preparation of CdS films at various substrate temperatures and in ultra-high vacuum is discussed. The possibilities of using molecular beam evaporation sources is also discussed.

TASK IV: ZINC OXIDE MATERIAL IMPROVEMENT

The difficulties in evaporation of zinc oxide are discussed and the results of these experiments are presented.

III. PUBLICATIONS, REPORTS, CONFERENCES

The content of the following papers is related to and in part derived from work performed under this contract:

"Thin-Film Active Devices," W. Tantraporn and K.K. Reinhartz, National Electronics Conference, Chicago, Illinois, October 8-11, 1962.

"Composite Analysis of Thin Film Active Devices," W. Tantraporn, Special Meeting of the AIEE Solid-State Circuits Committee, Seattle, Washington, August 23-24, 1962.

The following meetings were held between representatives of the U.S. Army Electronics Research and Development Laboratory and the Electronics Laboratory of the General Electric Company to discuss technical work under the subject contract:

a. June 27, 1962, at Syracuse, New York
b. October 22, 1962, at Fort Monmouth, New Jersey
c. January 7, 1963, at Syracuse, New York
d. March 26, at Fort Monmouth, New Jersey.

IV. FACTUAL DATA

Task I: Field Effect Triodes

4.1 Theory of Thin Film Field Effect Triodes

4.1.1 Introduction

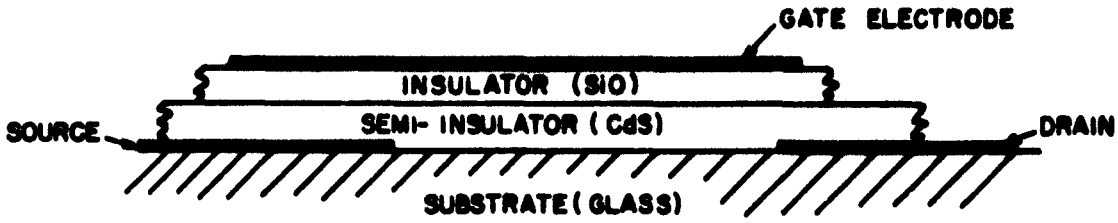
Thin film triodes having a geometrical arrangement similar to that shown in Figure 1 have been reported recently[1]. The materials used as the semiconductor layer allowing successful operation are CdS and CdSe. (Some other semiconductors including Si, Te, etc., have been tried, but with very limited success.) Although successful modulation of the source-drain current by the gate voltage is achieved, the physical mechanism of modulation has not been understood.

To summarize briefly the nature of the problem, only the results for CdS triodes will be used. (CdSe triodes exhibit similar characteristics*.) The characteristic curves of the triode performance can be classified roughly into two classes. Class (1), depicted in Figure 2 (often called the non-saturation type), shows appreciable source-drain current as a function of the drain voltage, and the influence of the positive or negative gate voltage is to increase or decrease the current with respect to the zero gate condition. Class (2), shown in Figure 3, exhibits saturation characteristic of I_{SD} as a function of V_{SD} and the effect of the gate voltage is an increasing function of the positiveness of the gate. Contrary to class (1) triodes, the class (2) triodes have negligible transconductance at lower or negative gate biases.

There have been at least three schools of thoughts on the mechanism of the modulation. The first and perhaps the most common mechanism or model is that of conduction via the surface charge accumulated under the insulator-semiconductor interface (cf. Figure 1) as the gate is biased positive. This mechanism is considered by Weimer[1], and its modified versions covering the class (2) type characteristic appear

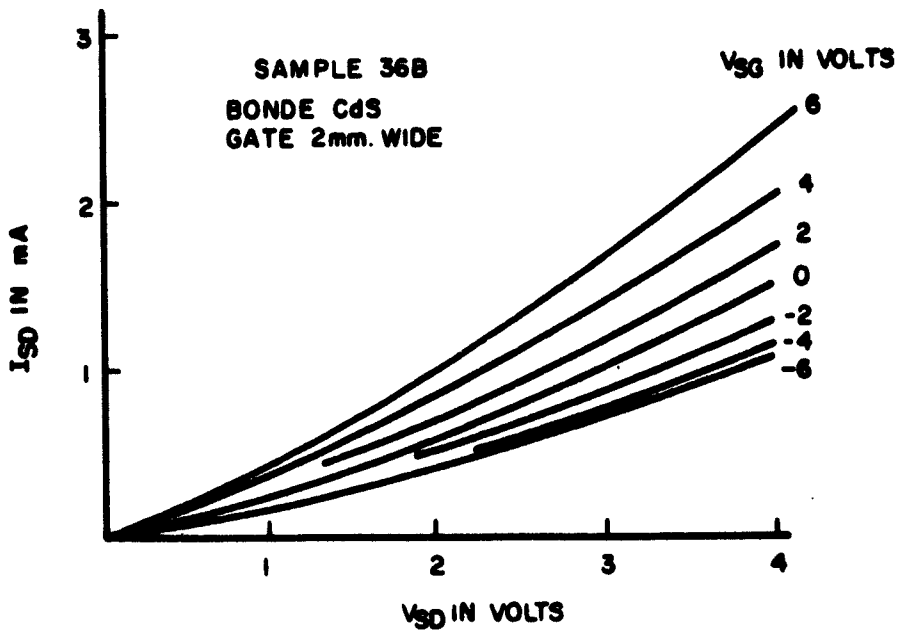
---

*For Electronics Laboratory samples only.



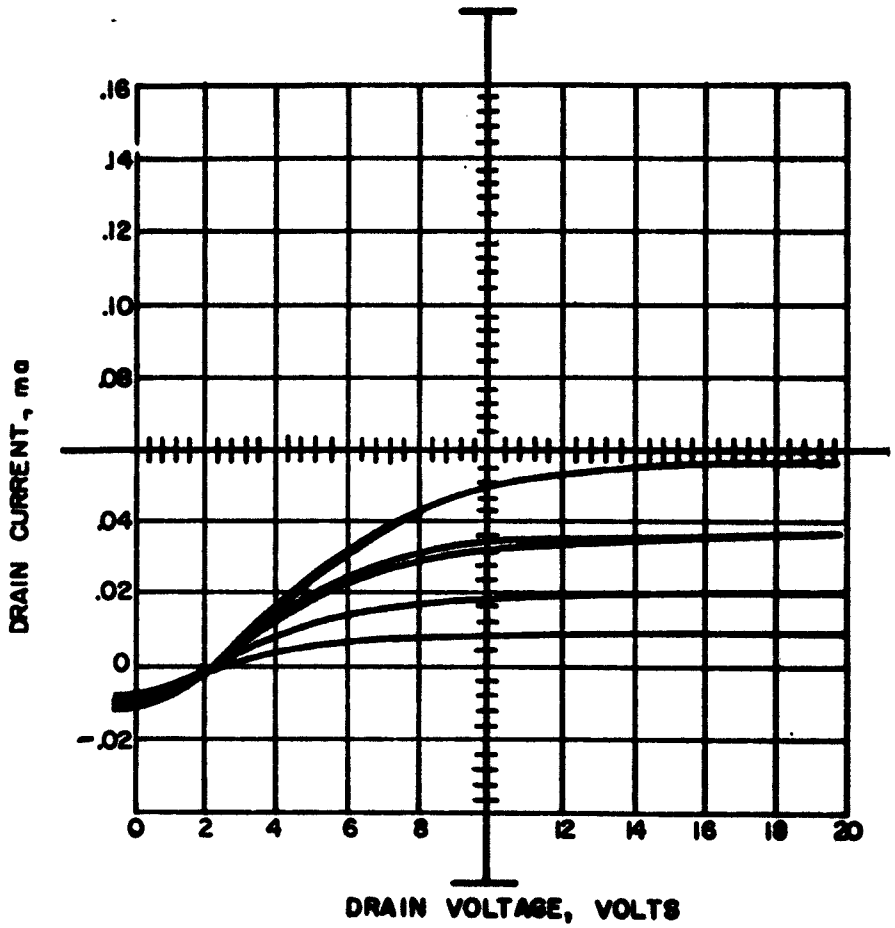
SCHEMATIC DIAGRAM OF THE THIN FILM TRIODES CONSIDERED

FIGURE 1



DC CHARACTERISTICS OF A CLASS I TRIODE. (THE WIDTH OF THE GATE SEEMS TO HAVE NO APPRECIABLE EFFECT)

FIGURE 2



DC CHARACTERISTICS OF A CLASS 2 TRIODE

FIGURE 3

elsewhere[2,3]. This mechanism was questioned by Tantraporn and Reinharts[4] since it does not fit certain preliminary experimental results.

The second model was advanced by Zuleeg[5] in an unpublished report. He proposed that the gate electrode, being closer to the source than the drain, exerts a much stronger field and pulls off space charges from the source electrode (if the source forms negligible barrier height with CdS) which are transferable to the drain. This mechanism would account for the saturation effect in samples in which the drain voltage has negligible ability to draw appreciable current. However, in the cases where the drain voltage can produce sufficient field to draw space charge current directly from the source, the insulated gate then merely modulates the space charge flow electrostatically similar to the space charge limited triode proposed by G.T. Wright[6].

Note that the mechanism proposed by Zuleeg requires the existence of strong gate fields in the CdS layer, whereas the Weimer type of mechanism requires interface charges, implying a very weak gate field in the CdS layer. Yet both mechanisms will yield algebraically the "saturation current" as being proportional to the square of the gate voltage[3,5]. (The square law holds approximately for the class 2 triodes.)

The third model was that advanced by Tantraporn[7] who considered the effect of the electric field due to both the drain and the gate on the barrier height (at the source electrode) or the trap-depth (within the CdS). The lowering of the activation energy required to overcome the barrier height or trap depth manifests itself as an increase in the current. This mechanism was thought to be important in view of the preliminary result of reference (4) and some data of reference (8).

This section will describe a sequence of experiments designed to establish the modulation mechanism in the CdS triodes of both classes. First, a complete set of experiments was performed on a class (1) triode, establishing the existence of a field dependent activation energy of the source-drain conduction. Similar experiments on the class (2) triode are not as conclusive, due to experimental difficulties inherent in this class.

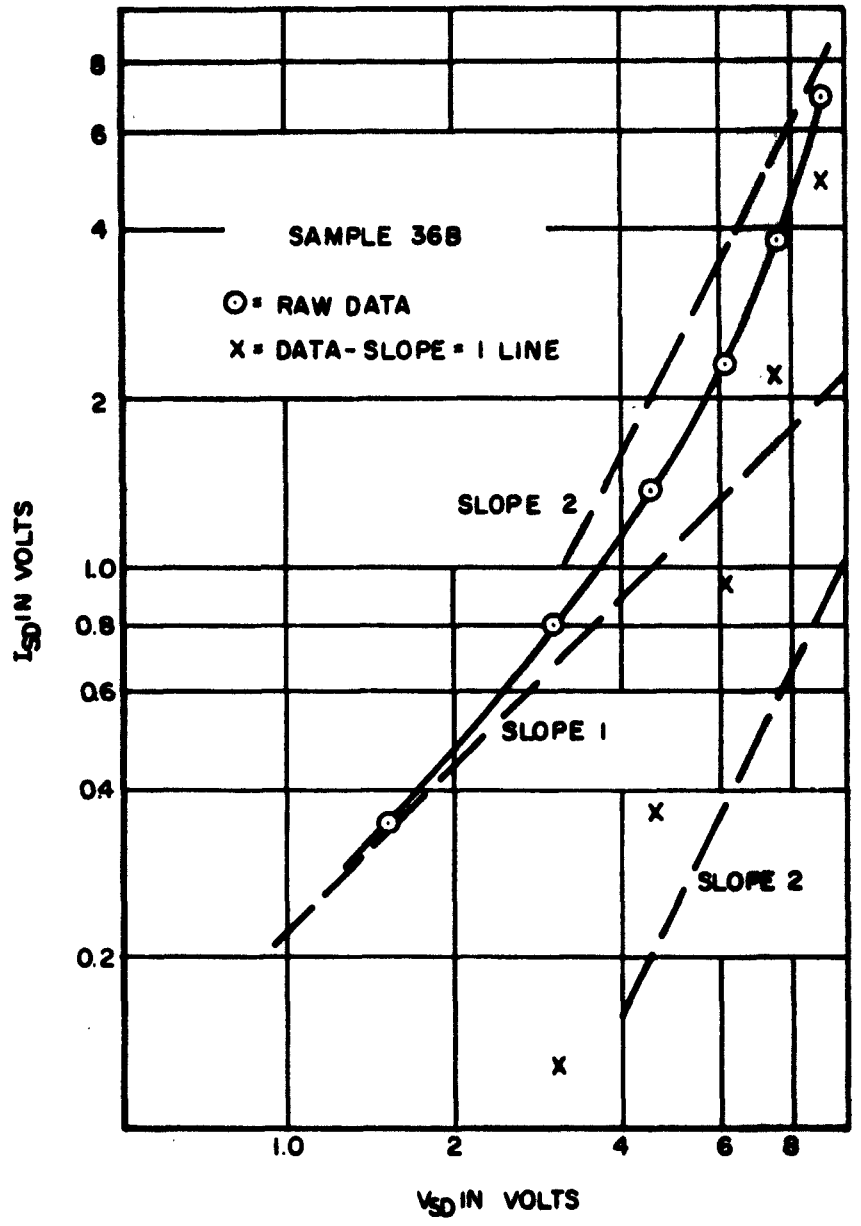
The measurements of the electric field of the gate as compared to the source-drain field showed that the gate field is much stronger in the class (2) than in the class (1) triode. It will be argued that the only mechanism that can explain the strange behavior found in the electric field experiment on the class (2) triode is the emptying of the excess space charge trapped in CdS. It is then shown that the trap emptying mechanism can be the modulation mechanism in both classes of triodes. Space charge injection is necessary, while the conduction channel mechanism may be the mechanism of drainage, all in the same modulation process.

4.1.2 Experiments and Interpretations on the Class (1) Triodes

As mentioned earlier, the class (1) triodes are those which at zero gate voltage exhibit supralinear dependence of I_{SD} on V_{SD} (see Figure 2). For a class (1) sample having a 15 μ masked separation between the source and drain, (the actual gap width is not known, and may not be regular) the current is of the order of 1 ma/cm-gap-length at 1 volt bias. In contrast, a class (2) sample under similar conditions would pass a current of the order of 1 μa/cm-gap-length, or an order of magnitude higher or lower.

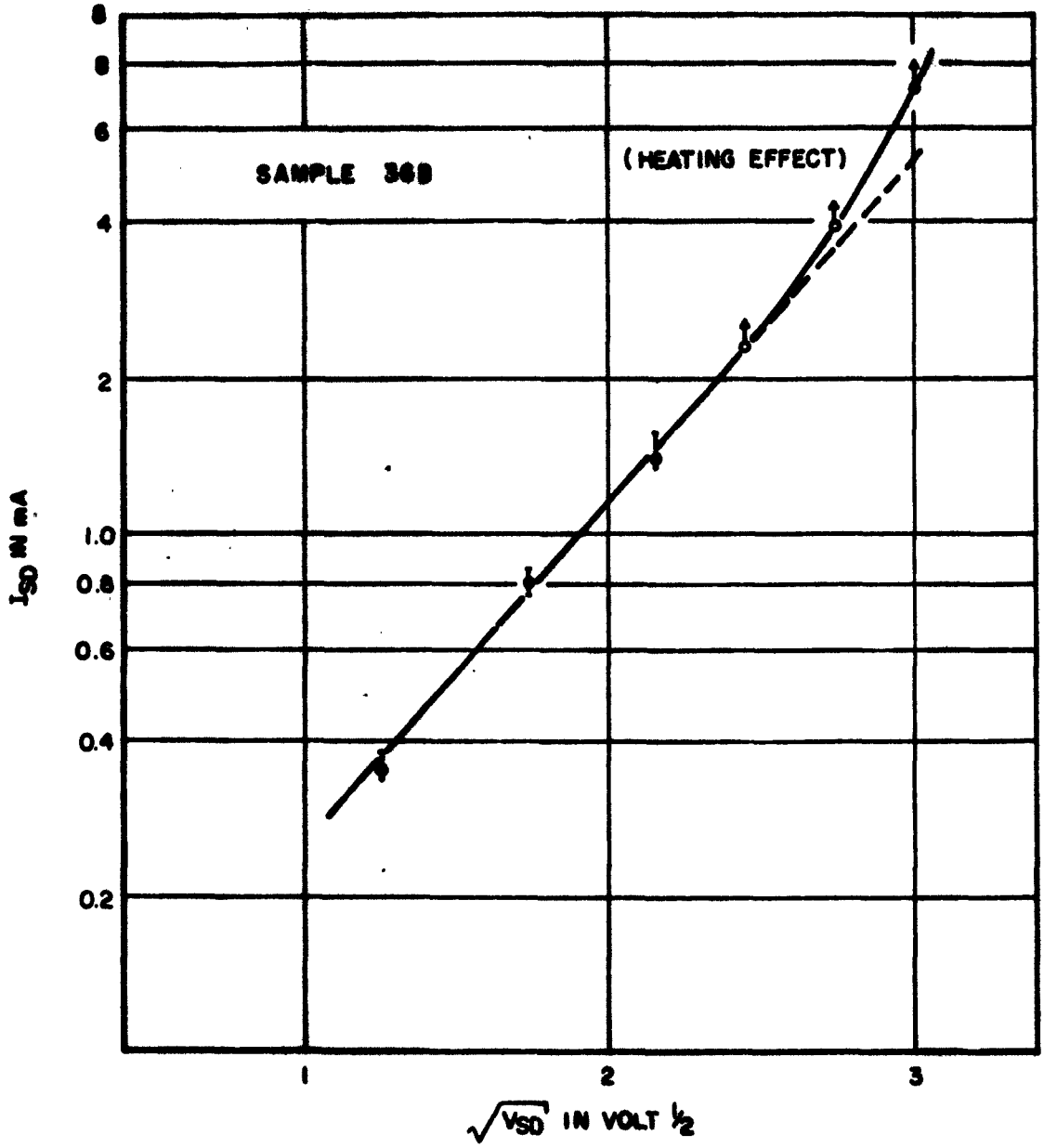
4.1.2.1 The Analysis of the Current-Voltage Relationship

In order to determine whether the supralinearity in the class (1) sample is due to the SCL current part as suggested by Zuleeg[5], the current-voltage curve I_{SD} vs. V_{SD} is replotted in the log-log scheme in Figure 4 where the net current (less the ohmic part) is also plotted. It may be seen that the SCL square law is not obeyed. When the data of Figure 4 is plotted in the log I vs. $\sqrt{V}$ scheme in Figure 5, however, the fitting is considered good. It is noted that the higher-voltage point ($\sim$9 volts) contains a heating effect (to be discussed later), which should cause the experimental current value to be too high. Such a heating effect is easily identified when the current increases as a function of time at



CURVE FITTING OF I_{SD} VS. V_{SD} SHOWING THE NON FITNESS OF THE FUNCTION $I = AV + BV^2$, i.e. OHMIC + SPACE CHARGE-LIMITED CURRENTS

FIGURE 4



PHENOMENOLOGICAL FUNCTION $I \sim e^{\beta\sqrt{V}}$ AND ITS FITTING TO THE EXPERIMENTAL POINTS. (POINTS ARE TRANSPLOTTED FROM DC RECORDER TRACE. ARROW SIZES QUALITIVELY INDICATE THE RATES OF DRIFT DUE TO HEATING.)

FIGURE 5

the constant high voltage*

The plotting scheme of Figure 5 is based on the relationship

$$I \sim e^{-\frac{1}{kT}(\psi - \beta\sqrt{V})} \qquad (1)$$

(where ψ is the zero-field activation energy and β is a constant) which arises in the case the current flow is limited by a barrier height[9]. Since the $V^{1/2}$ dependence arises when the barrier shape is coulombic, the same voltage dependence would be expected if the conduction process is by a space charge current limited by trapping due to some trapping centers[7] which may be represented by potential wells with walls described approximately by a coulombic function.

4.1.2.2 The Activation Energy as a Function of Applied Voltage

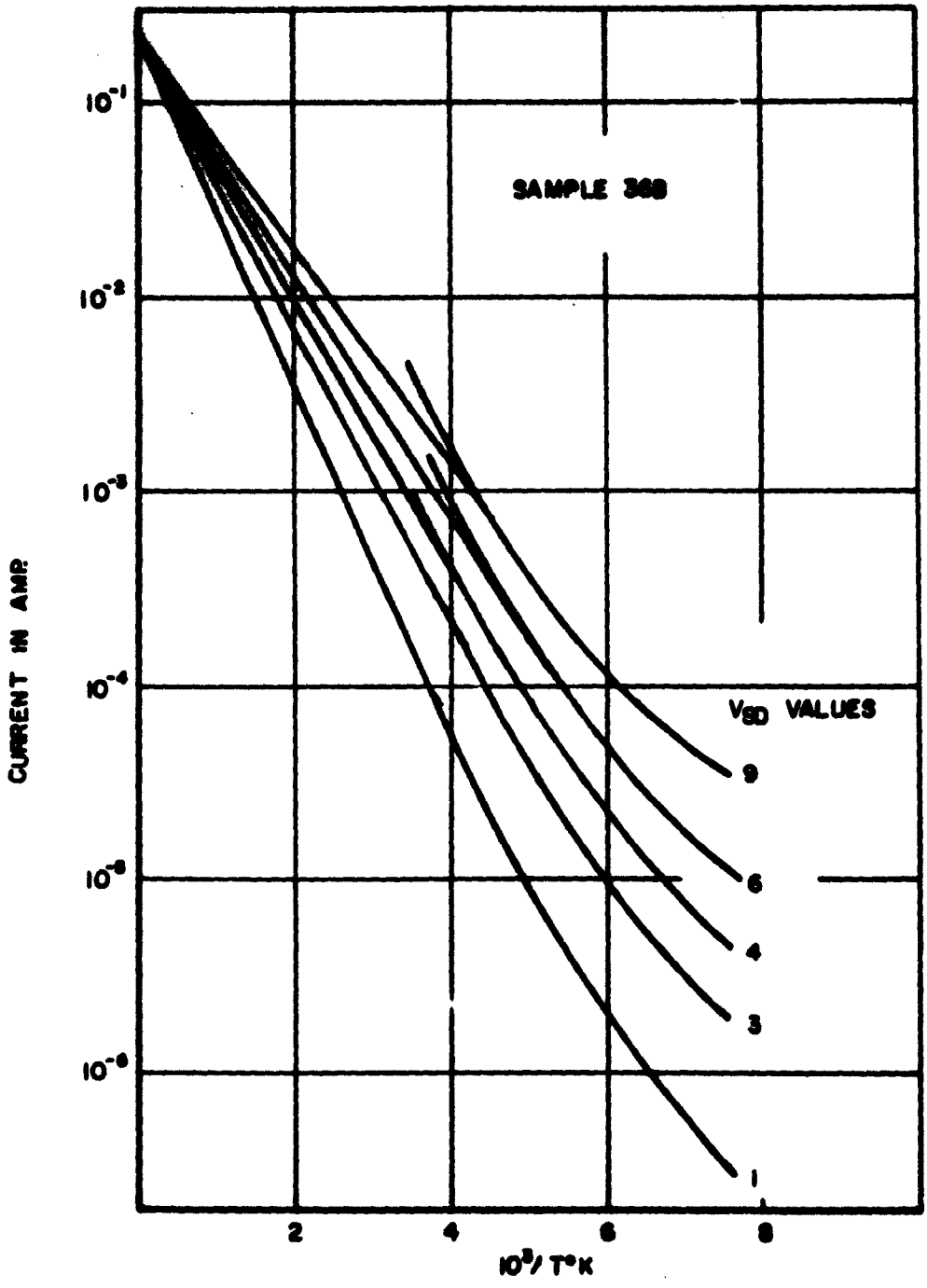
As a result of 4.1.2.1 that the current flow is limited by a process requiring an activation energy, it will be a good check to perform the temperature dependence measurement on I_{SD} at constant voltage values**. Sample 36B, whose data were used in the previous analysis, will be used throughout for consistency. (It must be pointed out that similar results have been obtained on other samples, but a complete set of measurements has so far been carried out on sample 36B only.)

Figure 6 exhibits the temperature dependence of I_{SD} at various constant values of V_{SD}, plotted in the log I vs $10^3/T°K$ scheme. The extrapolation of the straight lines to a common point at $T \to \infty$ was done by first extrapolating the V = 1 curve linearly to the ordinate. From

---

*Many independent experiments have been performed at the Electronics Laboratory to establish the joule heating effect in CdS film on glass. The temperature change of 100°C is not unlikely, and the initial rate of temperature change may be of the order of 10^{4}°C/sec.

**Temperature control apparatus was described for the glow curve experiment proposed in the 2nd Quarterly Report[7]. Here the sample is cooled down, then the temperature is let to approach room temperature or higher at a rate of 40°C/hr., approximately. For the highly conductive sample 36B the current value vs temperature is reproducible, and not different from the value when the heating rate is as low as the leak through the top plate of the vacuum thermos ($\sim$100°C/day).



TEMPERATURE DEPENDENCE OF I_{SD} AT VARIOUS V_{SD}

FIGURE 6

the ordinate, intercept lines are then drawn to be tangential to the curves at higher voltage values.

Similar results are shown in Figure 7 for the case $V_{SD} = V_{SG} = V$. It is noted that for a value of V_{SD} the current for $V_{SG} = V_{SD}$ case is always higher than the $V_{SG} = 0$ case, at any given temperature.

Linear extrapolation to a common intercept at $1/T = 0$ in Figures 6 and 7 is justified by two reasons.

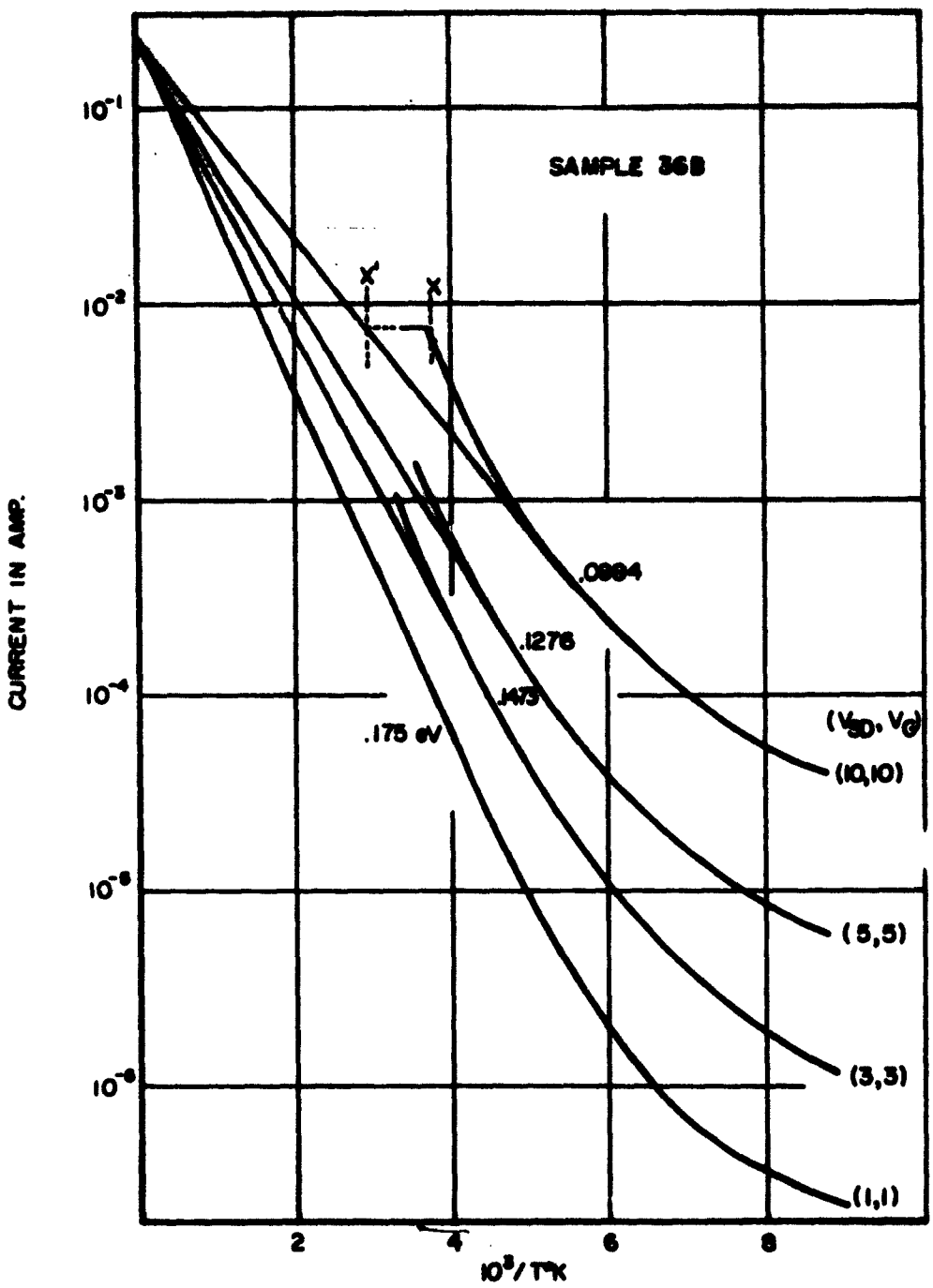
A. Experimental - Reference 8 presented similar experimental results with better straight fitting at lower values of $1/T$, presumably due to better thermal condition. We identified the deviations of the experimental points from the straight lines, especially at higher power level, as due to the heating effect by performing separate experiments (drifting of current, differently controlled thermal conditions, frequency dependence, etc.). The sacrifice in the non-fitting is traded off for the reproducibility of the results under the experimental conditions employed. Nevertheless, the activation energy calculated from such a plot is reliable at least for the low voltage cases.

B. Theoretical - The polycrystalline, non-stoichiometric, thin film of CdS used no doubt has enormous imperfection densities (chemical, surface and intergrain boundaries, lattice defects within the grains, etc.), and it is, therefore, justified to regard the deep lying levels (measured from the conduction band edge) as compensated and the interaction with the conduction band as dominated by those levels nearest to it. By the magnitude of the current observed in the class 1 triodes, the activation energy of the interaction must be rather small. If the source contact-barrier is sufficiently small*, then the electron density is given by[6]

$$n = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} e^{-E/kT} = N_c\, e^{-E/kT} \qquad (1)$$

---

*This assumption is necessary also in the mechanisms considered by references 1, 2 and 3.



TEMPERATURE DEPENDENCE OF I_{SD} AT VARIOUS $V = V_{SD} = V_{SG}$

FIGURE 7

provided

$$N_T \; e^{E/kT} \gg N_c \qquad (2)$$

where E is the activation energy,

N_T is the density of the local levels in exchange with the conduction band,

and other symbols have their usual meanings.

Since N_T is expected to be large for the film, and $E \gg kT$ even for the small E, condition (2) is quite safe as $N_c \sim 10^{19}$ cm^{-3}.

Since the mobility μ is known to be generally temperature dependent as $T^{-3/2}$, except at lower temperatures (cf. ref. 11 for single crystal CdS), the temperature dependence of the current reduced to

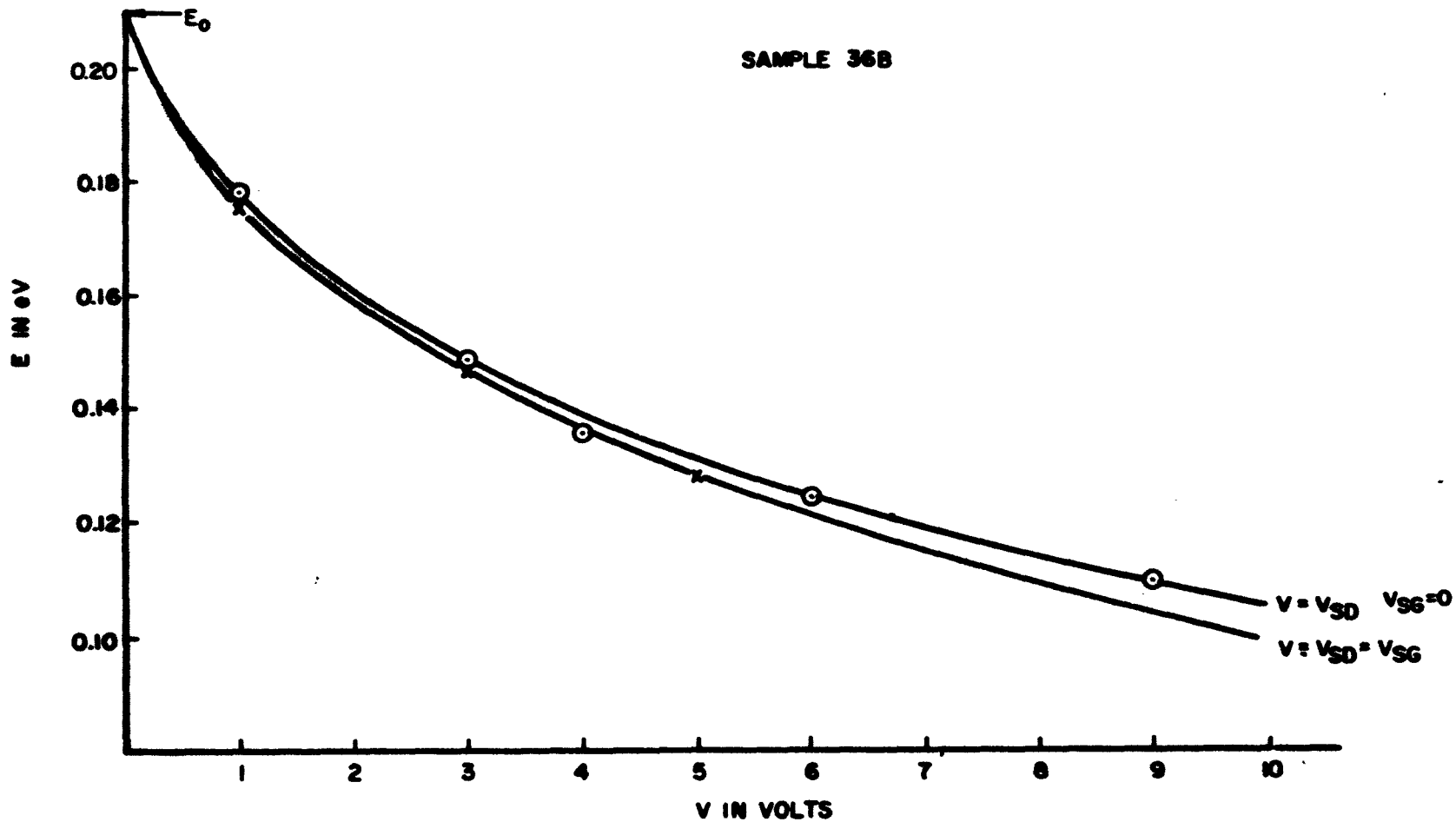
$$I \sim ne\mu \sim e^{-E/kT} = I_o e^{-\alpha x} \qquad (3)$$

where $\alpha = \frac{E \times 10^{-3}}{k}$ and $x = 10^3/T°K$. The $x = o$ intercept of current in Figures 6 and 7 determined by extrapolation of the low voltage case is, therefore, allowed as a basis for "interpolation" for the higher voltage cases.

The slopes of the lines in Figures 6 and 7, measured in eV, are plotted as a function of the voltage in Figure 8a, for both $V_G = 0$ and $V_G = V_{SD}$ cases. The extrapolation toward zero voltage suggests the activation energy of 0.21 eV, herewith defined as E_o. The reduction from E_o due to the applied voltage is then plotted as a function of $\sqrt{V}$ in Figure 8b, in order to check the barrier height modification effect $\beta\sqrt{V}$ in equation (1). The straight line drawn through the origin to best fit the points gives a slope

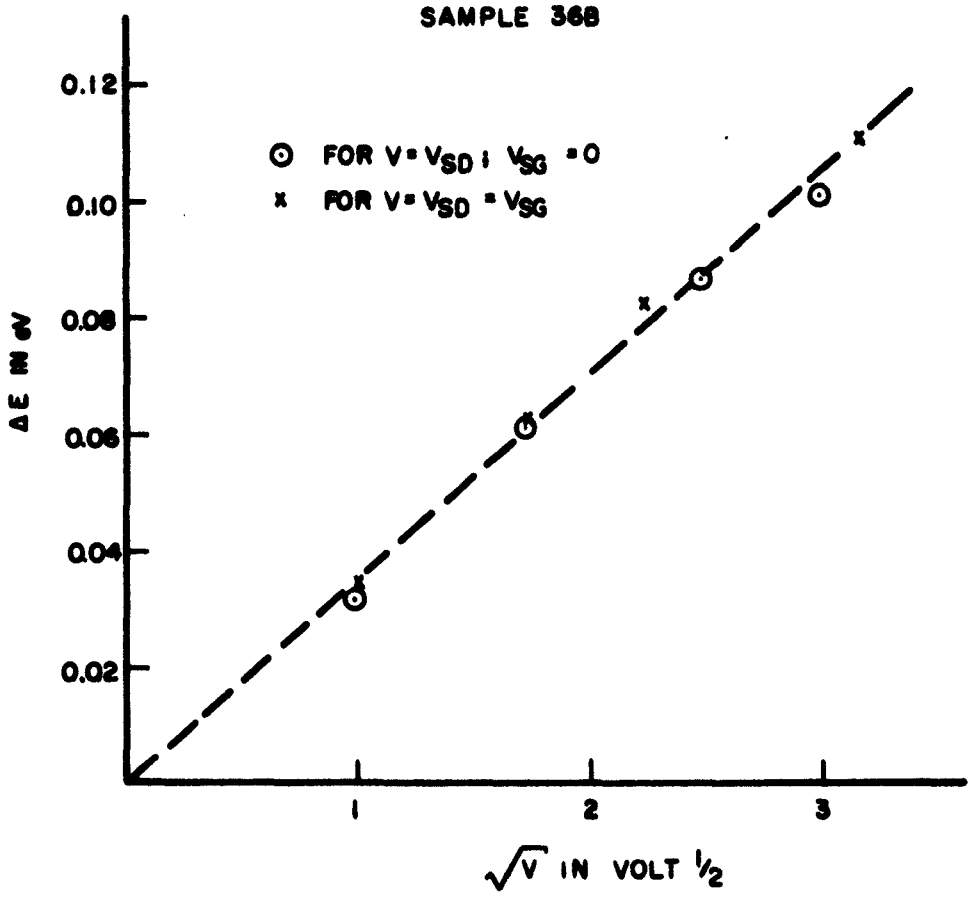
$$\partial E/\partial \sqrt{V} = 0.035 \qquad (eV)/Volt^{1/2} \qquad (4)$$

It is, therefore, no surprise to find that the activation energy found for other samples at $V_{SD} = 1.5$ volt is usually of the order of 0.16 ~ 0.18 eV.



THE ACTIVATION ENERGY E AS A FUNCTION OF VOLTAGES. (BOTH CURVES ARE DRAWN WITH THE SAME FRENCH CURVE, ROTATED AROUND THE POINT 0.21eV)

FIGURE 8a



TEST FITTING OF ΔE OF FIGURE 8a AS A FUNCTION OF $\sqrt{V}$

FIGURE 8b

The reduction of the barrier height by an electric field (the Schottky effect) is given theoretically by

$$\Delta E \text{ (in eV)} = 3.79 \times 10^{-4} \left(\frac{F}{\epsilon}\right)^{\frac{1}{2}} \qquad (5)$$

with F in volt/cm and ϵ in cgs units. For CdS, $\epsilon = 9$, so that comparison of (5) with (4) yields for this sample an equivalent distance d across which the voltage V is applied giving rise to the field F:

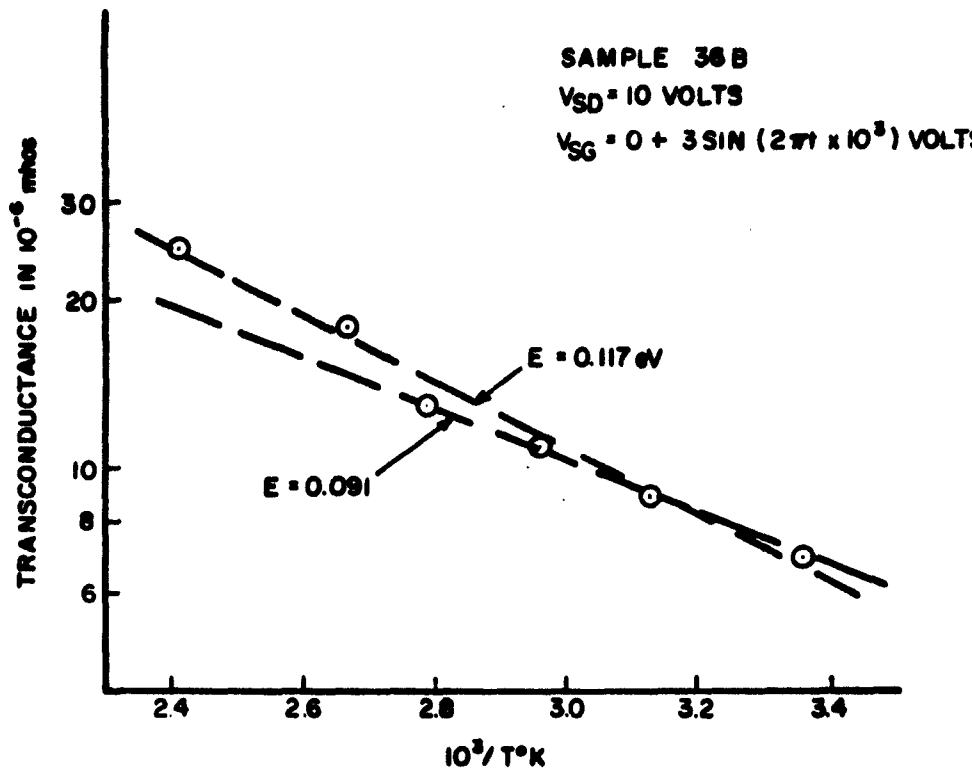
$$\text{(For sample 36B)} \quad d = \left(\frac{3.79 \times 10^{-4}}{3 \times 0.035}\right)^2 = 0.13 \times 10^{-4} \text{ cm} \qquad (6)$$

Since the gap between the source and drain electrodes is designed to be about 15 microns, the value 0.13 microns suggests either that the real gap of consequence is much smaller than the wire mask used, or that the voltage drop is across a barrier layer of 0.13 micron thick and the field is negligible elsewhere in the CdS film. Since there are no complete sets of measurements for other samples, the values of d have not been obtained for these samples for the purpcse of comparison with the sample 36B used.

For completeness sake the temperature dependence of the transconductance of the sample 36B has been measured between 300 and 415°K at $V_{SD} = 10$ volts, dc $V_{SG} = 0$, ac $V_{SG} = 3$ volts, 1 kc frequency. The result is shown in Figure 9. It is interesting to note that the value of the activation energy from the data is 0 105 $\pm$ 0.015 eV, to be compared with the data at 10 volts in Figure 8a.

4.1.3 Experiments and Intepretation on Class (2) Triodes

For the class (2) triodes many experimental difficulties were encountered in the attempts to perform measurements similar to those for the class (1) triodes. The difficulties stem mostly from the fact that at $V_{SG} = 0$ the current I_{SD} is very small at reasonable V_{SD}, so that measurements similar to 4.1.2.1 are not reliable. The temperature dependence measurements require heating rather than cooling the sample, and this markedly contributes to changes in the physical and electrical properties as a function of time. Only qualitative results can, therefore, be discussed here.



TRANSCONDUCTANCE VS. TEMPERATURE

FIGURE 9

For V_{SG}= 0, the I_{SD} drifts up at a given V_{SD}= const. The drift time is very long, of the order of hours. At sufficiently high V_{SG}= const, i.e., when I_{SD} is sufficiently large, I_{SD} drifts down after V_{SD} is turned on. The drift time is rather fast, of the order of seconds. At low V_{SG}, the drift up characteristic prevails.

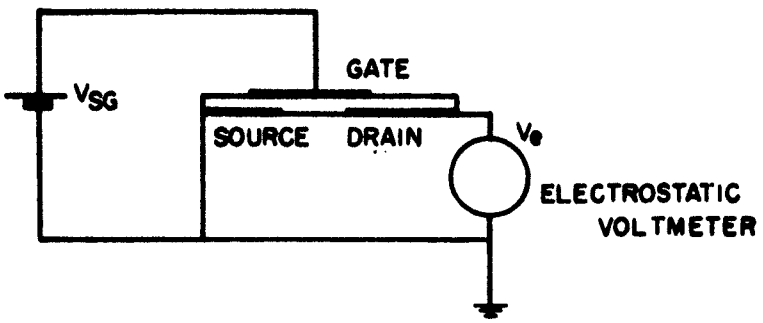
The conduction mechanism requires an activation energy of 0.2 eV or more.

The modulation as a function of temperature with a two-second gate voltage pulse seems to have a maximum. The maximum is at lower temperature for a higher gate voltage, for the range $\pm$ 80°C about room temperature. The temperature "position" of the maximum, however, coincides with the transition of "drift-down" (high temperature portion) and "drift-up" (low temperature portion) of I_{SD}, and thus may be fortuitous.

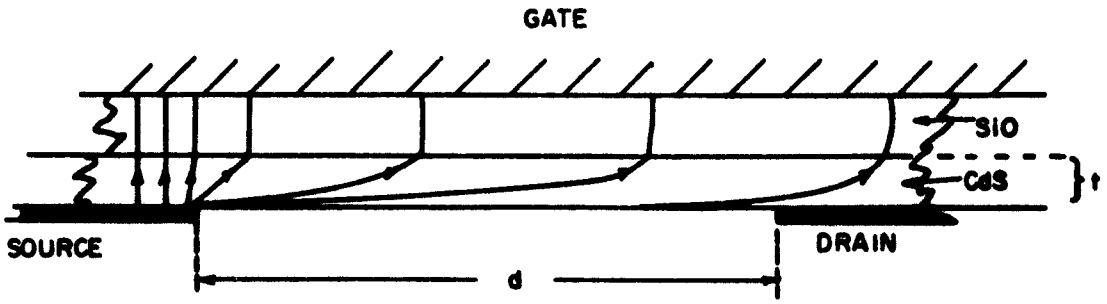
Interpretations on these experiments would be premature at this time. Some discussion will be made in connection with other experiments to be described later, however.

4.1.4 Semiquantitative Measurement of the Source-Gate Field

In order to aid in the interpretation of the experimental results and judge which reasonable mechanism could be operative, it is necessary to know, at least comparatively, the magnitude of the field in CdS due to the gate voltage. The experimental arrangement shown in Figure 10a would allow an estimate of this field. As the voltage V_{SG} is applied, there is a finite, but small, gate leakage current. The usual geometry of the triode is such that CdS thickness is about 0.5 μ, SiO thickness about 0.5 μ and the source-drain distance of about 10μ. The gate width is much larger than 10μ in practice, and so the gate can be considered as an infinite plane relative to the thicknesses and the gap width. Such is the case depicted in Figure 10b, where the electrostatic field V_e in Figure 10a arrangement would reach the potential $\left(\frac{d}{d+t}\right) \cdot V'_{SG}$ where V'_{SG} is the maximum voltage drop across any part of the CdS (provided $V'_{SG} < 1/2\ V_{SG}$), and d, t are the gap width and CdS thickness, respectively. Since usually $d \gg t$, V_e read in this experiment



(a)



(b)

FIGURE 10: (a) SCHEMATIC DIAGRAM FOR MEASUREMENT OF THE MAXIMUM GATE VOLTAGE DROP IN THE CdS LAYER

(b) THE SOURCE-GATE LEAKAGE CURRENT STREAMLINES (SCHEMATIC) (FOR $d \gg t$, V_e/t REPRESENTS THE ORDER OF MAGNITUDE OF THE GATE FIELD IN CdS NEAR THE SOURCE)

is the maximum voltage drop across the CdS layer when the gate V_{SG} is applied. $(V_{SG} - V_e)$ then is the sum total of the remaining voltage drop across the SiO layer and the interface SiO-CdS. The maximum field in the CdS layer, in the region between the source edge and the gate is, therefore, of the order of V_e/t when V_{SG} is applied.

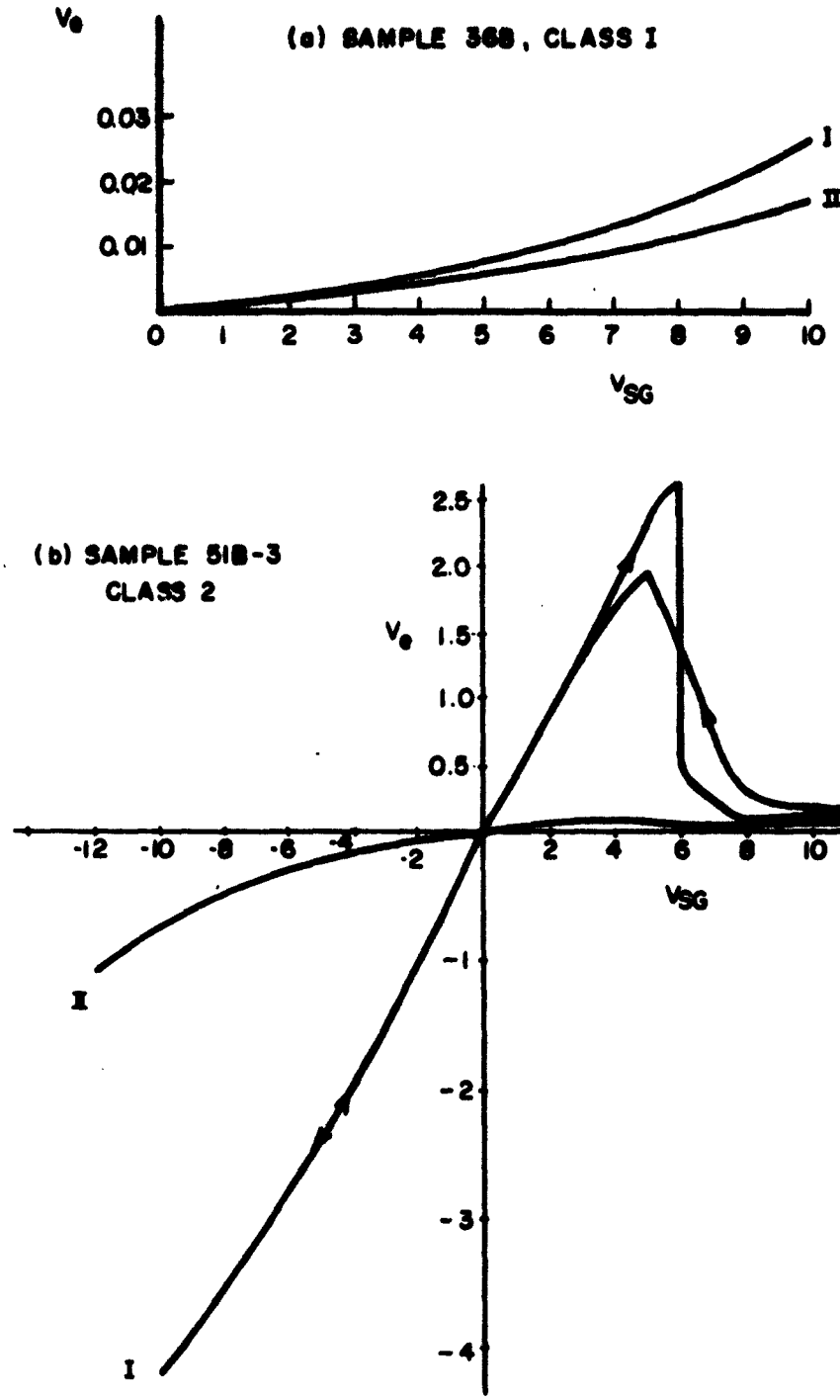
The values of V_e vs V_{SG} are plotted in Figure 11 for the class (1) triode (sample 36B), and a class (2) triode (sample 51B-3). The interesting feature in Figure 11b, namely, a negative slope region in the case $V_{SG} > o$, is common in all the class (2) triodes tested. It can be said from the testing of the class (2) samples (showing saturation characteristic of Figure 3) that the mechanism responsible for such negative slope behavior is probably also causing the saturation characteristic.

Writing $F_{SG\ max}$ in CdS as V_e/t and F_{SD} as V_{SD}/d for a first approximation, the ratio of $F_{SG\ max}/F_{SD}$ is, therefore, $V_e d/V_{SD} t$, or $\frac{cd}{t} \cdot \frac{V_{SG}}{V_{SD}}$ where c is the ratio V_e/V_{SG} obtained for data similar to those in Figure 11. Thus if $\frac{d}{t}$ ratio is 20 then c needs to be only larger than 0.05 in order to have in some region $F_{SG} > F_{SD}$ at the same applied voltages $V_{SD} = V_{SG}$. Therefore, a criterion of classification for the class (1) and (2) triodes can perhaps be stated as $F_{SG} < F_{SD}$ and $F_{SG} \gg F_{SD}$, respectively, for the same voltages applied. Note that from Figure 11b, V_e is almost 0.5 V_{SG}. If $\frac{d}{t} = 20$, the field ratio F_{SG}/F_{SD} for this sample can be as large as 10 at the operation point $V_{SD} = V_{SG}$. In a current-carrying case, however, the field ratio is a very strong function of position, and will be discussed later.

4.1.5 Overall Discussion of the Experimental Results, and Comparison with the Theories

From the experimental results described above, one may summarize the main points as follows:

(a) The conduction mechanism between the source and drain requires an activation energy. For class (1) triodes the activation energy is 0.21 eV. Correction for the heating effect is necessary at higher power



VOLTAGE DROP IN CdS AS A FUNCTION OF THE GATE VOLTAGE
I AND II DENOTES SOURCE-DRAIN POSITIONS INTERCHANGED

FIGURE II

density of Joule heating*.

(b) The activation energy, for class (1) triodes, is dependent on the applied voltages, in a manner closely approximated by $\Delta E \sim -\beta\sqrt{V}$.

(c) V_e obtained in the manner described above is very small compared to V_{SG} for the class (1) triodes, whereas it is not so very small in the class (2). Moreover, the class (2) triodes exhibit V_e anomally as V_{SG} is increased positively.

It is very instructive now to consider the fitness of the three theories on the modulation mechanism when applied to these experimental results. Of the latter we regard the experiment described in Figure 10 and the results in Figure 11b as most instructive. It must again be emphasized that the "anomally" in Figure 11b is common in all class (2) triodes, and not associated with breakdown.

Take first the theory of interface charges[1,2,3]. The situation described in Figure 10 would necessitate the monotonic increase of V_e as a function of V_{SD}. The dependence of V_e on V_{SG} via this mechanism may be supralinear, or saturation-like caused by shielding, etc., but will certainly not contain the anomally as in Figure 11b. It is also interesting to note that if the electric field in CdS between the source and gate is very high, then the interface charge density, defined by

$$\rho_s = \rho_{s_o} + \epsilon_1 F_1 - \epsilon_2 F_2 \qquad (7)$$

where ρ_{s_o} is the charge in the surface states, usually neglected or regarded immobile, and subscripts 1 and 2 are for the SiO and CdS respectively. Since $\epsilon_2 \sim 3\,\epsilon_1$ the mobile charges $(\epsilon_1 F_1 - \epsilon_2 F_2)$ will be very small if $F_2 \sim 1/3\, F_1$, or even would become of the wrong kind if $F_2 > F_1$ as might be possible, although unlikely, in a very high resistivity CdS.

In order to explain the anomally observed in this experiment on the class (2) triodes "excess" space charge injection and trapping in

---

*The critical Joule power level, of course, depends on individual thermal conditions.

CdS must be invoked, in such a way that the gate field in CdS will eventually cause space charge to accumulate in the region near the drain electrode in the experiment depicted in Figure 10a, decreasing the voltage drop (due to leakage current streamline in Figure 10b) reaching equilibrium near zero*. The mechanism by which this may occur follows.

One first notes that the experiment current in Figure 3 can be very large, and therefore, the current density is large, of the order of more than 1 amp/cm^2 when active area of the source electrode is taken into account. Such large current density can be drawn only when the contact barrier height source-CdS is not blocking, which is also the necessary assumption in the interface charge mechanism. The experiments described in 4.1.2.1 and 4.1.2.2, establishing the need for the modulatable activation energy will not explain the anomally observed as in Figure 11b, if the activation energy is assigned to the traps, however, then all the experimental behaviors can be at least qualitatively accounted for, as follows.

As the source-CdS contact is taken to be non-blocking, there will be, by diffusion, some space-charge free electrons in CdS in the vicinity of the source, creating an electric field against further increase of such diffusion. The space charges in this CdS region will be partly mobile and partly trapped. As the positive voltage is applied to the gate with respect to the source for a sufficient (short) time, the field in CdS maintained by the voltage drop along the leakage current streamlines allows more electron diffusion from the source into CdS. Now, as shown in Figure 10b, there is a positional gradient of the field strength ($\partial F / \partial x$) where F is the field and x is the distance along the source-drain direction. One may write

$$\frac{\partial n}{\partial x} = \frac{\partial n}{\partial E} \frac{\partial E}{\partial F} \cdot \frac{\partial F}{\partial x} \qquad (8)$$

---

*The equilibrium cannot be zero or negative, because the space charge is caused by the field which in turn is caused by the current streamline, whose voltage drop must remain positive.

where n is the mobile space charge density

E is the trap depth

F is the magnitude of the field, a function of position (x,y).

The existence of $\frac{\partial n}{\partial E}\frac{\partial E}{\partial F}$ has already been established (regardless to the physical nature of E) in Section 4.1.2. $\frac{\partial F}{\partial x}$ may be complicated algebraically, but its qualitative variation must be similar to that shown in Figure 10b. Thus $\frac{\partial n}{\partial x}$ must exist, giving rise to the diffusion current of space charges,

$$J_D = - e\mu kT \frac{\partial n}{\partial x} , \qquad (9)$$

if J_D can be drained off. Since the experiment is designed as in Figure 10a, such migration is stopped when the electrons accumulate sufficiently at the "drain" electrode to oppose such flow. Such electron accumulation depresses V_e and keeps it low as observed.

Since the SiO undoubtedly forms a blocking contact against the gate electrode, such space charge anomally cannot occur when V_{SG} is negative.

The flow of the space charge along the negative density gradient builds up the electrostatic field against further flow. Therefore, the field in the bulk of CdS as discussed above is correct only at the instant of voltage application. For example, the electrons trapped in the region between the source and gate, when freed, will travel to the CdS-SiO interface and hence cancel the field. This is the reason why when there is no drain voltage, the circuit of Figure 10a cannot produce current in the source-drain circuit at constant V_{SG}, as the charges accumulated on the boundaries of CdS cancel the internal field completely. If, however, one considers the possibility of indefinitely maintaining such "instantaneous" field configuration by properly injecting and draining out the driven charges, then one can say that the "saturation" current of the class (2) device occurs when the drainage is just enough to maintain the field configuration. Further increase in drain voltage will not increase the current if most of the voltage drop is near the drain (see below).

Figure 12 depicts the "saturation" case, i.e., when $\frac{\partial n}{\partial x}$ is caused by the gate field while the source-drain field is taken as negligible in such gradient-creation. This approximation holds, as may be seen later, except near the positive drain. Since the current density*

$$J_x = ne\mu F_x - e\mu kT \frac{\partial n}{\partial x} = J_F + J_D \qquad (10)$$

(where $\frac{\partial n}{\partial x}$ is taken as due to V_{SG}, F_x is taken to be due to V_{SD}) is to be continuous, i.e., independent of x, (cf. Figure 12c) the component field current J_F must be equal to $J - J_D$ or

$$J_F = ne\mu F_x = \text{const} + e\mu kT \frac{\partial n}{\partial x} \qquad (11)$$

in such a way that F can be obtained by dividing $J_F(x)$ by $n(x)$. (See Figure 12d.)

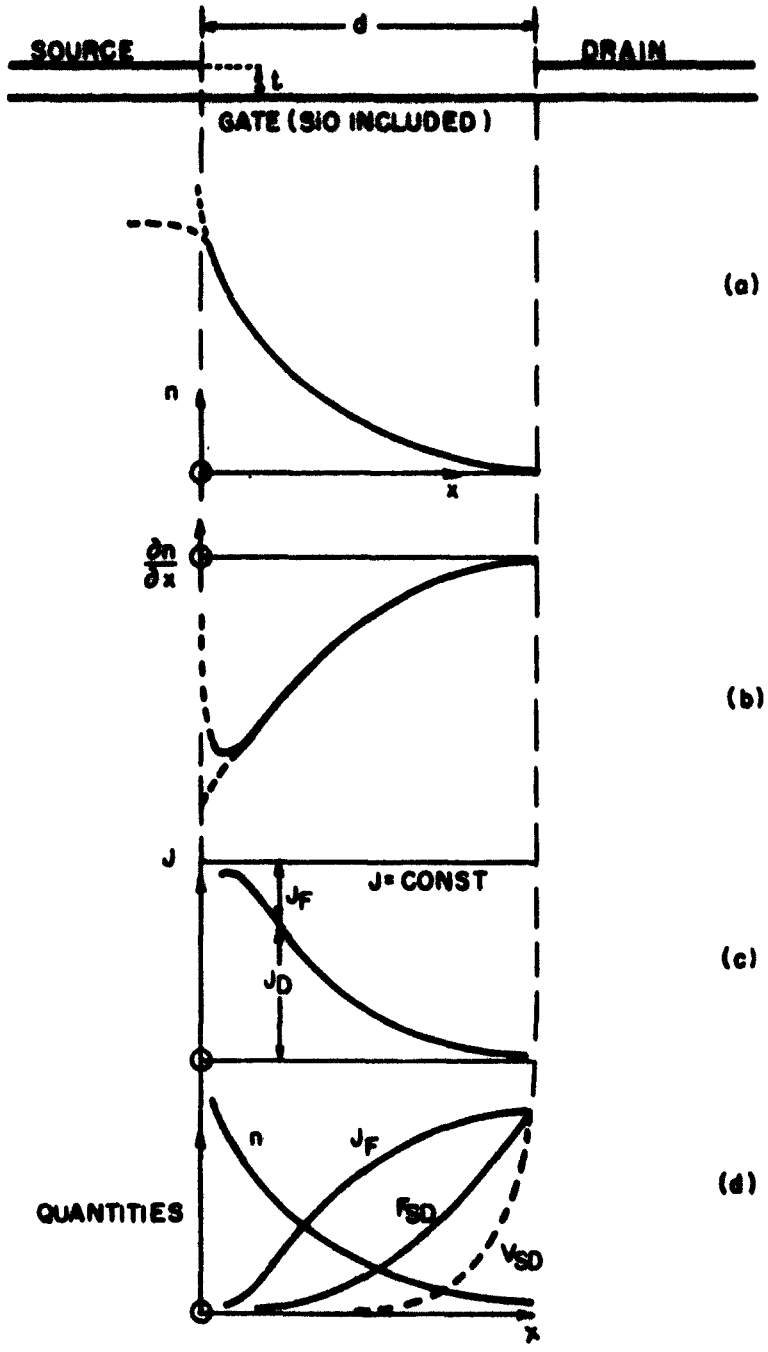
It is noted that if the diffusion current is a rapidly varying function of position, then the source drain field is strong only near the drain justifying the saturation criterion assumption, since an increase in V_{SD} will apply itself to the low charge density-high field region. At some point the current is almost totally carried by the diffusion term. It is, therefore, of interest to calculate the magnitude of the diffusion current near its maximum value.

The field due to the gate $F_y = F_{SG} = f(cV)$ is regarded as in the direction normal to the film (valid when $x > t$, the CdS film thickness) so that from conformal mapping[10] one obtains

$$F_y = \frac{V}{t} \left(1 + 3\, e^{2\phi}\right)^{-\frac{1}{2}} \qquad (12)$$

---

*e and μ are both taken as positive numbers.



QUALATATIVE EFFECT OF J_D ON J_F , F_{SD} AND V_{SD} AS A FUNCTION OF POSITION

FIGURE 12

where ϕ is related to x by

$$x = \frac{t}{\pi}(\phi + e^{\phi}); \tag{13}$$

$V_{(x)}$ is the voltage at the SiO-CdS interface, assumed constant.

It is easily shown that for large x

$$\frac{\partial \sqrt{F_y}}{\partial x} = \sqrt{\frac{V}{4\sqrt{3}\cdot x}} \qquad x^{-\frac{3}{2}} \tag{14}$$

Now writing the mobile excess charge density in equilibrium with the shallow traps as*

$$n(x) = N_c\, e^{-E(x)/kT}, \tag{15}$$

one finds

$$\frac{\partial n}{\partial x} = \frac{\partial n}{\partial E}\,\frac{\partial E}{\partial \sqrt{F}}\cdot\frac{\partial \sqrt{F}}{\partial x}$$

$$= \frac{3.79 \times 10^{-4}}{2\sqrt{\epsilon x}\sqrt{3}}\;\frac{N_c}{0.0258}\;e^{-\frac{0.21}{0.0258}}\cdot e^{\frac{3.79\times 10^{-4}}{0.0258}\sqrt{\frac{V}{\epsilon\pi\sqrt{3}\cdot x}}}\cdot x^{-\frac{3}{2}}\, V^{\frac{1}{2}} \tag{16}$$

where $\frac{\partial E}{\partial \sqrt{F}} = 3.79 \times 10^{-4}\,\epsilon^{-\frac{1}{2}}$ has been used (equation 5), and T = 298°K. N_c may be taken as 10^{19} cm^{-3}.

Note that according to (16) $\frac{\partial n}{\partial x}$ dependence on x has no maximum.

---

*cf. 1st Quarterly Report:

$$n = \frac{N_t N_c}{N_c + N_t e^{E/kT}}$$

where N_t and N_c are the trap density and the conduction band density of states, respectively, and E the trap depth. Now if $N_t \cdot e^{E/kT} \gg N_c$, true when $N_t \gg 2.9 \times 10^{15}$ cm^{-3} at room temperature for E = 0.21 eV, then equation (15) is valid. For a strong field case when E = 0.1 eV, N_t must be much greater than 2.1×10^{17} cm^{-3} for eq. (15) to hold. Since for polycrystalline thin film N_t may be of the order of 10^{19} or 10^{20} cm^{-3}, eq. (15) appears to be quite safe.

This is because we use the condition $x \gg t$. Since $\frac{\partial \sqrt{F}}{\partial x} \rightarrow o^*$ as $x \rightarrow o$ and negative, there must be a maximum at some $x > o$. The calculation of the position of this maximum is very tedious, and so for an order of magnitude calculation it is reasonable to assume that the maximum of J_D is near $x = t$. If so the charge density gradient becomes

$$\left(\frac{\partial n}{\partial x}\right)_{max} \sim \frac{-9 \times 10^{18}}{\sqrt{\epsilon}} \; e^{0.63\sqrt{\frac{V}{t\epsilon}}} \cdot \frac{1}{t}\sqrt{V/t} \text{ cm}^{-4} \qquad (17)$$

if t is expressed in microns. With an assumed (near experimental) value of $\mu \sim 0.9$ cm^2/volts-sec., and electrode edge of 0.3 cm along the gap, the "saturation" current at room temperature is approximately

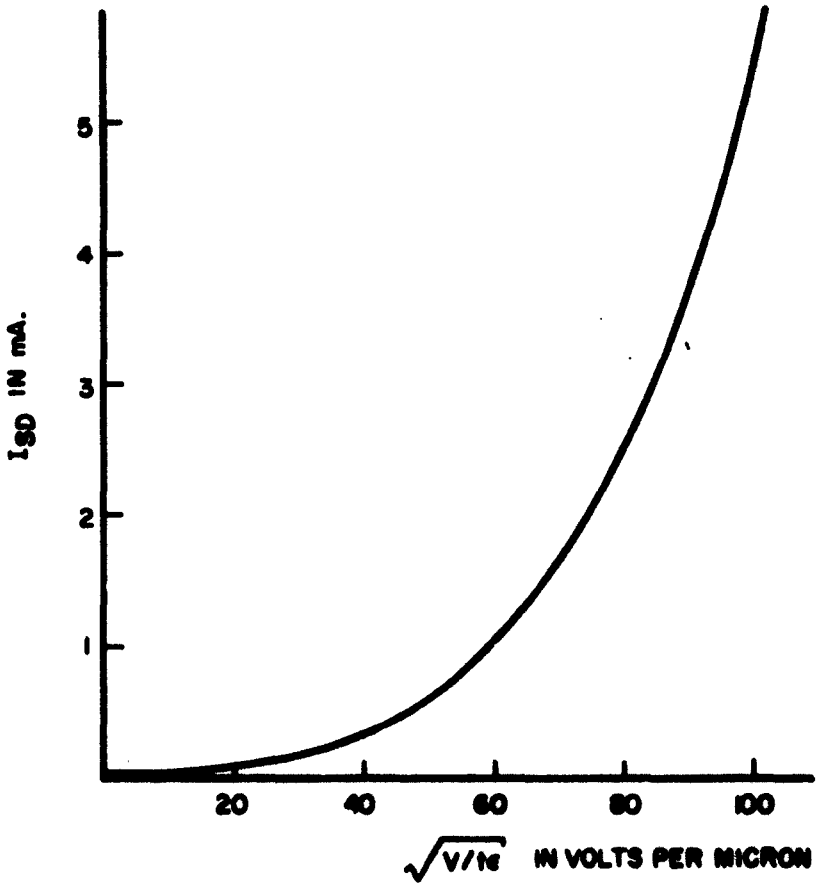
$$I_{SD} \sim 10^{-6} \; e^{0.63\sqrt{V/t\epsilon}} \cdot \sqrt{V/t\epsilon} \text{ amp} \qquad (18)$$

The "saturation" source-drain current for this "common" class (2) triode is plotted against the CdS equivalent field $V/t\epsilon$ in Figure 13. Note that V is the voltage drop across the CdS layer between the source and the gate due to a gate voltage V_{SG}. V may be of the order of a small fraction of V_{SG} (see Figure 11).

Equation (18) may exhibit I_{SD} vs V similar to the square law if $V/t\epsilon$ is in the range near unity, and would fit log I vs $\sqrt{V}$ scheme if $\sqrt{V/t\epsilon}$ is much larger than unity, as used in Figure 13. It may even follow $I \sim V^{1/2}$ scheme if $\sqrt{V/t\epsilon}$ is very small. Generally, the saturation current (cf. Figure 3) occurs when $V_{SD} \sim V_{SG}$. The experimental results for the

---

*From the conformal mapping standpoint alone. Actually the electrons in the source do diffuse thermally into the CdS region $x \sim o$ regardless of the field, and the value $\frac{\partial n}{\partial x}$ in CdS may not have a maximum. It is thought that the field F should merely go to zero as x approaches zero (cf. Figure 12d). In such a case the estimate of the saturation current by (17) should perhaps have used an equivalent $x < t$ value for the assumed maximum. By lumping $t\epsilon$ together, however, we combine the two uncertain quantities as one. The d.c. dielectric constant of CdS is usually 9, but for Schottky type expression, ϵ is merely an unknown effective dielectric constant in the atomic range.



SATURATION SOURCE-DRAIN CURRENT AS A FUNCTION OF THE MAXIMUM FIELD IN THE CdS LAYER

FIGURE 13

class (2) triode usually show that the saturation current I_{SD} (at $V_{SD} = V_{SG}$) is dependent on V_{SG} in a manner similar to that shown in Figure 13, i.e., faster than $I \sim V^2$ type dependence.

In the approximate derivation of the saturation current given above, no consideration is given to the source drain distance other than that the diffusion current is a rapidly decreasing function of x (cf. equation 16). The criterion for saturation to occur is also vague. Here then the conducting channel along the interface of CdS and SiO layers may come in as the drainage mechanism, since the charges freed from the traps will originally drift toward the interface under the influence of F_y. This drainage mechanism yields saturation[2] at $V_{SD} = V_{SG}$, and the field configuration in the region near the drain must differ from the case considered above. However, the magnitude of the I_{SD} is limited by the trap emptying process in series with such channel conduction. Since the field configuration near the source is not much affected by the drain mechanism, the magnitude of the saturation current given by equations (15) (18) should still hold. Exact treatment on this subject will be left for the future, in order to yield the device design of the class (2) triodes.

For class (1) triodes, Figures 2-8 show that if the trap model is adopted, then apparently the drain voltage exerts the trap emptying influence, while the small field due to the gate (cf. Figure 11a) merely adds vectorially to the field of the drain. Since the trap emptying depends on the magnitude of the field, the modulation can be affected by both positive and negative gate bias. It turns out that at $V_{SG} = 10$ volts, $V_e = cV_{SG}$ of sample 36B (Figure 11a) is about 0.026 volt, so that the field is 520 volts/cm for the CdS layer of 0.5 μ thick. Such a field would contribute to a change of the barrier height by slightly less than 0.003 eV. This should correspond to the differences in the 2 curves of Figure 8a at V = 10 volts. Inspection shows that such is affirmed.

4.2 Design and Fabrication of Field Effect Triodes

4.2.1 Wire Masking of the Source Drain Gap

The wire masking technique is now the standard method of formation of the source-drain gap. Most working devices are made using 15 micron wire to mask a gap approximately the same width. However, the technique has been refined to permit the handling and use of wire 2.5 microns in diameter and production of similarly sized source-drain gaps. Devices utilizing source-drain gaps of these dimensions have been produced but the experimental results obtained from these devices indicated that this fine spacing does not produce the increase of transconductance expected from theoretical considerations.

4.2.2 Deposition and Control of Insulating Layer

The insulation layer used in device fabrication had been six minima in the intensity of reflected green light ($\sim$ 8000 Å) of silicon monoxide deposited in two layers at different temperatures to enhance both its adherence and insulation properties. It was felt from theoretical considerations that decreasing the insulation layer thickness would produce significant device improvement. Due to the malfunction of the optical monitor, no precise method of controlling film thickness during deposition was available. However, a program utilizing visual observation of color changes as a method of controlling thickness was instituted to determine the effect of decreasing the insulation thickness.

All devices made in this test had the CdS layer deposited at 800°C source temperature, 300°C substrate temperature, and 30 minute time of deposition. The results of this experiment are shown in Table I.

These results show an obvious improvement in device performance as the SiO thickness is decreased. Although the values of dc transconductance are not greatly improved over devices seen in the past, the ac transconductance of these samples is substantially above any observed at this time. More complete data on these devices are given in the measurements section of this report. Another noticeable change in the device characteristics is seen in the current-voltage curves. As the SiO is made thinner the device tends to

be more saturating. It was also found that these thinner SiO films retained their insulating properties and adherence was a less critical factor.

TABLE I

Device Properties vs Insulation (SiO) Thickness

Color Changes	Thickness (Approx.)	Transconductance DC	Transconductance AC	I-V Characteristics
4	5400Å	50-100 μmho		non-saturating
3	4100Å	100 μmho		non-saturating
2	2700Å	1000 μmho	400 μmho	saturating
1	1350Å	1500 μmho	625 μmho	saturating

4.2.3 Deposition and Control of CdS Layer

The effect of thickness of the CdS layer on device performance was also studied. For this series of devices the SiO thickness was held constant at two minima in the intensity of reflected green light (~ 2700Å) one deposited at 300°C substrate temperature and the other at 150°C.

At the beginning of this test the only monitor of CdS thickness was the time of deposition, which was generally set at 30 minutes. It was felt that thinner CdS would achieve better results so first experiments were carried out by decreasing the deposition time. Also it was found that color changes could be observed for this material. This method of monitoring thickness was used for later experiments.

First experiments were carried out at 300°C substrate temperature, but it was found that raising the substrate temperature to 350°C increased the device output resistance by a factor 10 and generally improved the device characteristics. The results of these experiments are shown in Table II.

The results shown are not felt to be conclusive due to changes made in the deposition equipment and positioning of the monitor. Also the thickness of those devices monitored only by timing is somewhat in doubt. These experiments are being repeated and more complete information for the 350°C substrate temperature is being obtained.

TABLE II

Device Properties vs CdS Thickness

CdS Thickness	Substrate Temperature 300°C				Substrate Temperature 350°C			
Time or Color Changes • Å	R_D, at $V_g = o$	Transconductance μmhos DC	AC	I-V Characteristics	R_D at $V_g = o$	Transconductance μmhos DC	AC	I-V Characteristics
30 min.	1×10^4	1000	400	sat.	3×10^5	1200	900	sat.
15 min.			250	non-sat.	3×10^5	600	350	sat.
10 min.	5×10^4	300	300	non-sat.				
8	1×10^6	5	12	sat.				
6	3×10^6	3	10	non-sat.				
4	4×10^5	10	30					
2	5×10^6	4	10					

4.3 Measurements on Field Effect Triodes

4.3.1 Measurement of the Characteristics of Field Effect Triodes

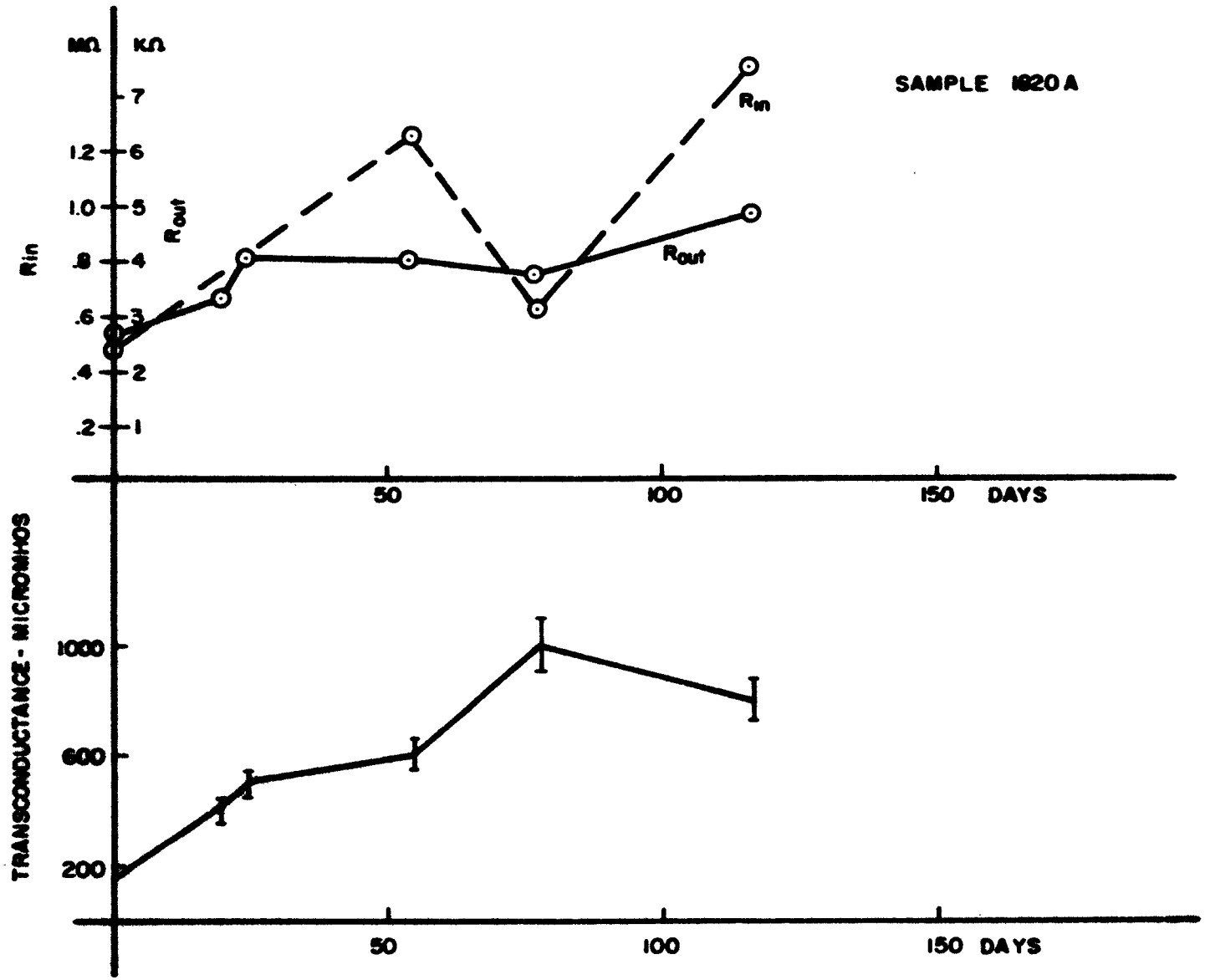
The measurement of the ac characteristics of field effect triodes as described in 4.3.1 of the Second Quarterly Report is very accurate and realistic as the triode is tested in an amplifier circuit. The ac characteristics can be determined over a wide range of operating conditions and signal frequencies, but the measurements are very time consuming and the results cannot be recorded automatically. For a fast routine testing of field effect devices one of the Tektronix curve tracers seemed to be more suitable. The electron-tube curve tracer type 570 probably will fit our requirements better than the transistor tester type 575 as the 570 will deliver voltage steps for the gate directly, has a wide range of load resistors, and allows higher biasing of the gate. The dc bias at the gate has to be measured externally, however. The steps of the gate voltage are produced by a saw tooth generator with a frequency of 120 cps.

As shown in Figure 3 of the Second Quarterly Report the transconductance of a typical field effect device is about constant at frequencies between more than 100 cps and the cut-off region. Therefore, the curve tracer should display the true ac characteristics of the device. This was confirmed by experiments.

The Tektronix curve tracer type 570 seems to be the most suitable tester for routine measurements of the drain family, transconductance, input and output impedance at one frequency. It eliminates the need for a dc tester, but the test circuit described in the previous report is still necessary if the frequency dependence of the device characteristics is of particular interest.

4.3.2 Time Stability of Thin Film Triodes

The dc characteristics of one typical field effect device, the source-drain resistance r_o without gate bias, the gate resistance r_{in} and the transconductance at an arbitrary operating point $V_D = 4$ volts, $V_G = 7$ volts were measured over 120 days. The results are given in Figure 14.



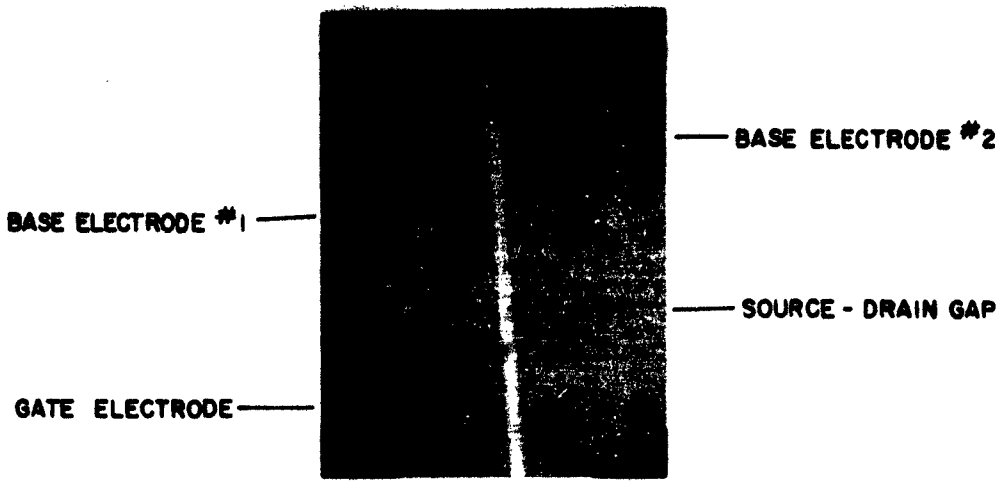
AGING DATA ON A FET
FIGURE 14

The data taken after 78 days are very irregular in all respects. If these data are neglected one can say all examined properties increase with time, the rate of change decreasing after the first 25 days. This behavior may be obtained assuming an annealing process which improves the structure of the CdS film. Simultaneously, favorable annealing of the SiO layer takes place as indicated by the reduced conductivity of this layer.

The study indicates that the characteristics of our field effect devices do not deteriorate within 4 months, but improve. As it is most desirable to have stable characteristics, the effect of an accelerated annealing of the device at elevated temperatures should be investigated in the future.

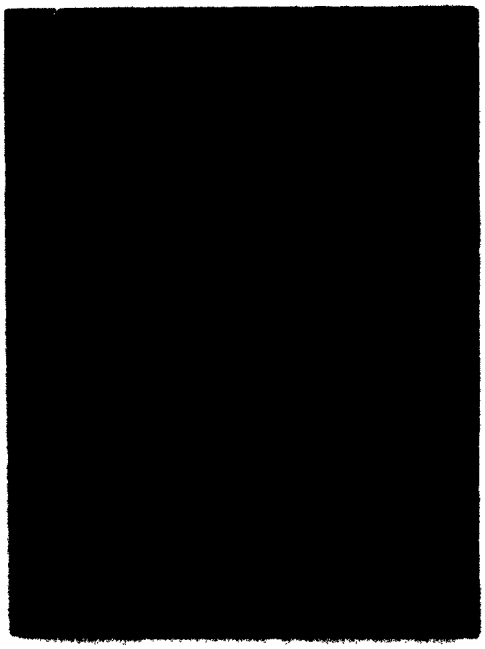
4.3.3 Effect of Electrode Configuration on the I_D - V_D Characteristic

In our typical thin film device the gate electrode is 3 or 4 times wider than the gap between the source and drain electrodes. The gate electrode can be aligned symmetrically or non-symmetrically with respect to this gap. In a symmetrical arrangement source and drain electrodes are interchangeable without change in the characteristic of the device arrangement. This is not true for a non-symmetrical arrangement. The effect depends on the degree of non-symmetry and is particularly pronounced in samples which show saturation of the drain current. Figures 15 and 16 represent an extreme case. Figure 15 shows a photograph of the device. The gate is 4 times wider than the gap and extends from one edge of the gap over the other edge. The drain characteristics of the device are shown in Figure 15 . In Figure 16a the gate extends over the drain electrode. The device shows a low transconductance of about 5 micromhos, but a good saturation of the drain current. Figure 16b shows the drain family for the reversed source-drain polarity. The transconductance increased to 25 μmho but the dynamic drain resistance dropped.



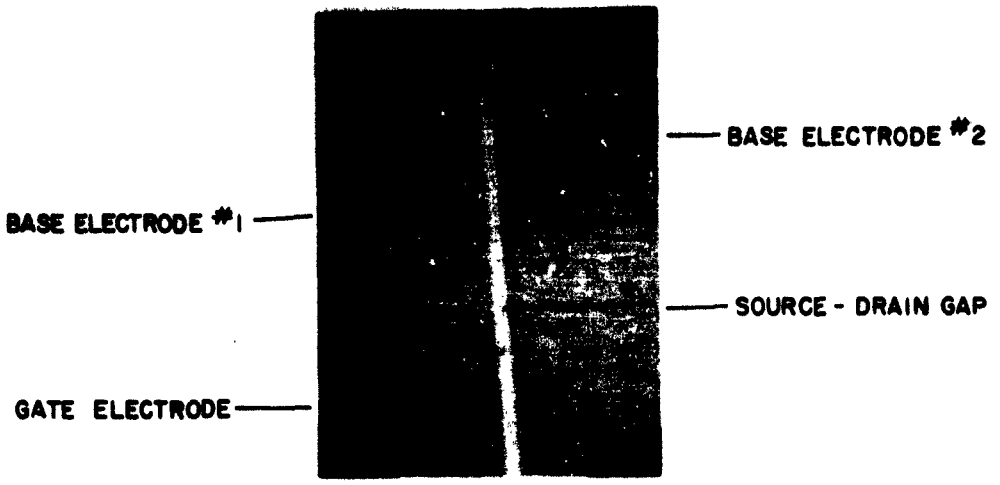
PHOTOMICROGRAPH OF FIELD EFFECT TRIODE GATE
AND SOURCE-DRAIN GAP

FIGURE 15



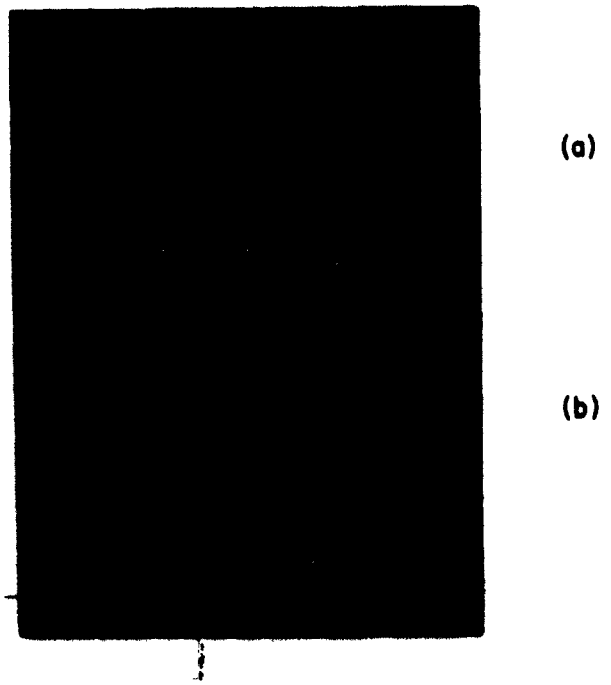
DRAIN CHARACTERISTICS OF A FIELD EFFECT TRIODE

FIGURE 16



PHOTOMICROGRAPH OF FIELD EFFECT TRIODE GATE
AND SOURCE-DRAIN GAP

FIGURE 15



DRAIN CHARACTERISTICS OF A FIELD EFFECT TRIODE

FIGURE 16

Task II: Space Charge Limited Triodes

4.4 Theory of Space Charge Limited Triodes

In previous reports, we have examined the one dimensional mathematical expressions relating space charge limited current to the applied voltage in the simple plane parallel electrode sandwich configuration. The result of these calculations is that the space charge limited current is proportional to the square of the applied voltage. In order to experience a strict dependence on the square of the applied voltage, it is necessary to fulfill several physical requirements.

When this subject was discussed before, these requirements were stated as guidelines to the development of a space charge limited triode. Experimental work performed during the last reporting period has yielded results which are a measure of the extent to which these requirements are being fulfilled. Let us consider them in the order in which they were originally taken up.

First, it was necessary to assume that the spatial variation of the fields in the dielectric would be such that no diffusion current would flow due to gradients in the concentration of free carriers. Although it is reasonable to assume no carrier diffusion in the usual plane parallel electrode geometries, a case has been found in a sample made in the field effect triode geometry in which diffusion of space charges appears to play an important role. This configuration and the measurements and their interpretation are treated in considerable detail elsewhere in this report. Therefore, only the essentials need be repeated here.

The most striking experimental result is obtained when a positive voltage is applied to the gate with respect to the source and an electrometer is connected between source and drain, allowing a potential measurement at impedances which are essentially open circuit. As the gate is slowly made more positive, the source-drain potential experiences a time dependent as well as a voltage dependent change which can most plausibly be explained in terms of a diffusion limited space charge current. Its importance for space charge limited triodes consists mostly of being an

illustration of a case in which this requirement was not fulfilled.

Second, there was a requirement that the electrical field must vanish at or near the surface of the source. This requirement may be stated in another way: The source contact must be ohmic. The contact must be ohmic in the sense that it must be able to supply an excess of electrons ready to enter the semiconductor whenever they are needed. The charge density and field in the neighborhood of the source should be similar to those encountered in the thermionic emitter of a vacuum tube operating under space charge limited conditions.

Although semiconductor technology in general, and experience with cadmium sulfide crystals in particular suggested ways of achieving ohmic contacts, there was some question about achieving these contacts in evaporated polycrystalline cadmium sulfide films. It is well known that surface states in semiconductors produce wide variations from the theoretically predicted barriers at metal-semiconductor interfaces. Experience is now showing that contacts made either by evaporating metals onto cadmium sulfide films or cadmium sulfide onto metal films are more likely to produce ohmic contacts than they are to produce blocking contacts. For example, contacts made to cadmium sulfide with indium, gold, cadmium, or chromium all make equally good ohmic contacts. Thus, this obstacle to achieving space charge limited currents seems to have been easily overcome.

Third, there was a requirement that the ohmic current, that is, the current of carriers in thermal equilibrium with the conduction band must be negligible compared to the space charge current. This is equivalent to the requirement that the transition time for space charge current across the sample must be small compared to the dielectric relaxation time. It was shown in an earlier report that this requirement places a lower limit of 10^6 ohms/cm on the resistivity of the cadmium sulfide.

Many disappointing results have been reported earlier and attributed to inability of some of our vacuum systems to achieve the necessary high resistivity of the cadmium sulfide. This was particularly

disappointing in an all-glass evaporating chamber which had previously achieved resistivities well above this value. The malfunction of the glass system has now been traced to the gradual bridging of a thermocouple feed-through by stray deposits of cadmium sulfide. After this defect was corrected, the glass system was again capable of producing high resistivity films. More or less coincident with this improvement was the development of an indirectly heated and closely baffled crucible type source for CdS. This source operating in a metal vacuum system with glass bell jar also produces high resistivity cadmium sulfide. It thus appears that conceptually and experimentally, conditions are right for another advance in space charge limited triodes.

4.5 Design and Fabrication of Space Charge Limited Triodes

4.5.1 Materials

The materials used in constructing space charge limited triodes during this period were essentially the same as those used in the previous reporting period. Cadmium sulfide was used exclusively as the semiconductor material, silicon monoxide as the insulation layer, composite chromium and gold films as source and drain electrodes, and gold alone as the gate electrode. In addition, experiments were performed in which other source and drain electrode materials were used: Indium, chromium, and aluminum.

As was mentioned above the low resistivity of cadmium sulfide film was gradually overcome and continued experience with the indirectly heated crucible source resulted in better cadmium sulfide films. Better control in substrate temperatures and resistivities in a range suitable for space charge limited triodes were eventually achieved although too late to make any important contribution to device work in this period.

We have demonstrated that source and drain electrodes of different materials can conveniently be made by electroplating a second metal on one electrode of a source-drain pair, deposited simultaneously. This method was used in a number of experiments to plate one electrode with indium, leaving the other electrode of chromium and gold alone. By

interchanging the function of source and drain between these electrodes, it was possible to prove that gold and indium electrodes are equivalent in contact with our evaporated CdS.

In a similar experiment aluminum source and drain electrodes were deposited and one of these was then anodized in an effort to create a blocking layer. The results were somewhat confusing in that the anodized aluminum electrode was a lower resistance source than the unanodized aluminum electrode.

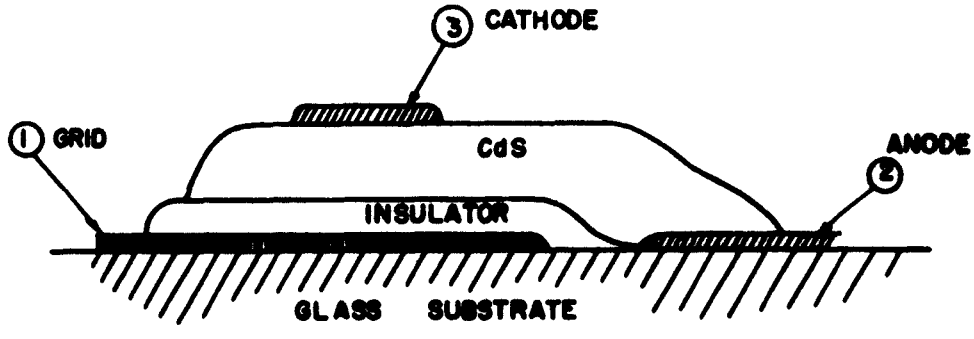
It is anticipated that the plating approach can be used for making single tellurium or selenium electrodes to get a blocking layer at the drain. A blocking contact at the drain has been found in the past to enhance the relative magnitude of the SCL current by suppressing the ohmic current.

4.5.2 Space Charge Limited Triode Configurations

During the first third of this reporting period, work was continued on the "simplified" space charge limited triode configuration shown in Figure 16 of the Second Quarterly Report and repeated here in Figure 17 for reference. After a reasonable amount of effort it was decided that this configuration is excessively difficult to achieve for mechanical reasons. Misalignment of the gate insulation layer and of the cathode accounted for failures in nearly every unit that was constructed. Accordingly, it was decided to make the space charge limited triodes with the same electrode configuration normally used for the field effect triode.

Being aware now of the difficulties encountered in achieving high resistivity cadmium sulfide, the results of this change to the field effect triode configuration can be anticipated. Many active devices were made but all of them operated as field effect triodes. As field effect triodes they were respectable devices showing saturation and some of them with transconductances in the enhancement mode of about 250 micromhos.

It was on this type of device that experiments were carried out using different materials in the source and drain electrodes leading to the conclusion that indium, chromium, or gold make equally good source electrodes. Also it was found that an anodized aluminum electrode was a better source



SIMPLIFIED CONFIGURATION OF SPACE CHARGE LIMITED TRIODE

FIGURE 17

than an unanodized aluminum electrode although aluminum electrodes are higher resistance emitters than the other metals.

Thus, while the late achievement of the means for making high resistivity cadmium sulfide interferred with making a working space charge limited triode, it was still possible to carry out meaningful experiments and to make some progress toward a successful device.

4.6 Measurements on Space Charge Limited Triodes

For the reasons stated above no genuine space charge limited triodes were produced during this period. The devices produced actually performed in the field effect triode mode and were evaluated along with the other field effect triodes.

Task III: The Improvement of Cadmium Sulfide Films

4.7 Post-Deposition Treatment of Cadmium Sulfide Films

This approach to the production of CdS films having properties suitable for field effect triodes consists of heating the deposited film in an atmosphere of hydrogen or hydrogen sulfide or a mixture of the two.

The purpose of such a treatment is the oxidation of excess cadmium or the reduction of excess sulfur in the CdS film, as may be required by the composition of the deposited material. The relatively low resistivity of the films deposited and the orange color of the films indicates that we are concerned with films containing excess cadmium, so that initial tests of the effect of post-deposition treatment have been carried out in a pure hydrogen sulfide atmosphere.

The experimental arrangement for the H_2S treatment of the films is pictured in Figure 18 . The purpose of the thermocouples at various positions along the furnace tube is twofold:

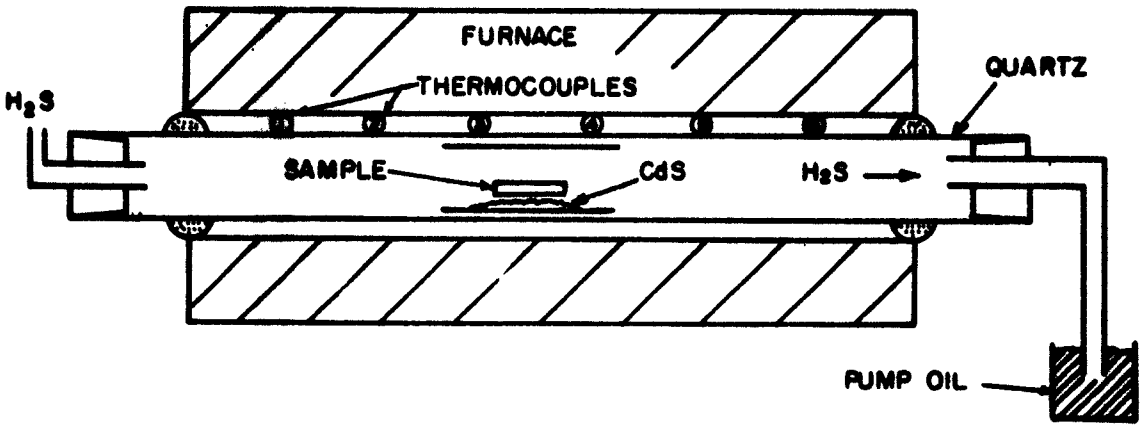
1. A knowledge of the temperature variations through the furnace allows the estimation of the temperature of each sample when several samples are treated simultaneously.

2. When runs are made in which incoming gas is saturated with CdS, it will be important to know how to arrange the saturating source and the sample under treatment so that a net loss or gain of CdS on the sample is not brought about.

The inner quartz tube containing the sample was used so that samples could be positioned relative to each other and relative to any CdS powder introduced and then the whole unit placed in the long quartz tube. This procedure is much easier than attempting to introduce all these things directly into the long quartz tube.

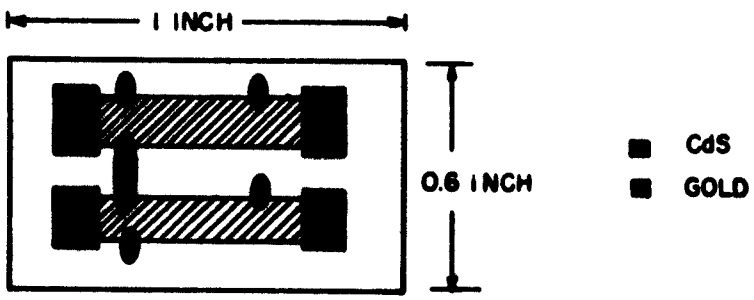
The exit tube for the H_2S enters a pool of Welch pump oil to avoid back diffusion of air, especially when the H_2S flow is slow (about 30 cc/min).

Samples for post-deposition treatment were made in duplicate pairs so that it might be determined whether the presence of gold contacts



EXPERIMENTAL ARRANGEMENT FOR POST-DEPOSITION TREATMENT OF CdS FILMS

FIGURE 18



SAMPLE CdS FILMS WITH GOLD CONTACT ELECTRODES

FIGURE 19

on the CdS during the post-deposition treatment (at 500-600°C) would have any large effect on the film. The tests were carried out as follows: (See Figure 19).

1. Two CdS films were deposited simultaneously on a pyrex substrate.

2. Gold contact electrodes were evaporated on one of the films (designated the "a" film) and electrical measurements were made on that film.

3. The pair of films was post-deposition treated; gold contact electrodes were then evaporated on the second film (the "b" film) and electrical measurements were made on it to determine the effect of the treatment. Finally, a and b were compared with each other after the treatment.

No evidence was found that the gold electrodes affected the film during the high temperature treatment. Of course, no effect was expected to show up with the configuration as shown in Figure 19 . This does not prove that there is not short range gold contamination of the CdS which would become significant in devices, where one is concerned with dimensions of a few microns. The possible short range diffusion of gold in CdS at 500 - 600°C will have to be determined in further experiments.

At present it has been established that the H_2S treatment of the CdS film is capable of raising the resistivity by a factor of about 10^4. In the first runs, mobilities increased during the treatment from about 1 to 12-18 cm^2/volt sec. In later runs the mobility did not change considerably, and we believe that the earlier phenomenon may have been due to the presence of traces of indium solder on the substrates which acted as a source of indium and brought about doping of the film. It does not appear at present that the high temperature H_2S treatment in itself was responsible for the increase in mobility.

Table III presents the available data on cadmium sulfide films before and after post-deposition treatment. Samples 6, 30, and 44 were single CdS films as in Figure 14 in the First Quarterly Report. The others are double samples as shown in Figure 19 of this report. The

TABLE III

Sample	Source T	Substrate T	mm. Hg P	Deposition Time	Before Treatment ρ	Before Treatment μ	After Treatment ρ	After Treatment μ
6	800	-	2×10^{-6}	30 min.	80	2	3×10^{5}	18
30	800	300	2×10^{-6}	" "	10^{6}	<1	19	12
44	800	100	2×10^{-6}	" "	22	2	10^{6}	<1
2a	800	150	4×10^{-6}	" "	4×10^{5}	<1	10^{10}	<1
2b	800	150	4×10^{-6}	" "	-	-	10^{8}	<1
6a	775	125	1×10^{-6}	" "	4×10^{3}	<1	(Broken film)	
6b	775	125	1×10^{-6}	" "	-	-	10^{8}	<1

letters a and b refer, respectively, to the film measured before heat treatment and the one measured only after heat treatment. The mobilities listed as less than one were too small to be determined with the apparatus presently available.

The pre-treatment electrical measurements were made on samples 6, 30, and 44 by soldering fine copper wire to the gold electrodes with tin-indium solder. The leads were then removed by scraping the solder away with a sharp blade. Some solder remained on the sample when it was put in the quartz tube for treatment, and it is very possible that indium and/or tin doping took place. The pre-treatment measurements on 2a and 6a were made with the aid of a special holder with gold plated spring fingers which made contact with the gold electrodes on the sample. No solder was used until after the post-deposition treatment. The effect of tin or indium doping will be tested during the next quarter, since the data give some indication that such doping may enhance the properties of the CdS.

4.8 Preparation of Cadmium Sulfide Films

4.8.1 Preparation of Films with Variation of Substrate Temperature

The relation between preparation parameters of CdS films prepared in the glass vacuum system and device characteristics was studied further. The results are given in Table IV . The thickness of the CdS films varied between about 0.5 and 1 micron The electrical characteristics were measured with a Tektronix curve tracer Model 570. In Figure 20 the ac transconductance of triodes taken from Table IV together with data from Table 3 (page 28) of the Second Quarterly Report are plotted as a function of substrate temperature during the CdS deposition. Assuming that the low values are due to a fault in sample preparation and the best values are characteristic, these are connected by a curve which then represents the transconductance as a function of substrate temperature. An important figure of merit for an active device is the voltage gain μ which is defined as $\mu = g_m \times r_o$, r_o being the dynamic drain resistance. The dynamic drain resistance of several samples is plotted as a function of CdS substrate temperature in Figure 21. It seems to be impossible to correlate these data, but even in the most favorable case the calculated voltage gain would be less than 10. Therefore, the preparation of CdS devices in the glass system was interrupted in order to accelerate the work in the new UHV system.

4.8.2 Evaporation in the Ultra-High Vacuum System

During this reporting period a new Ultek ultra-high vacuum system with stainless bell jar equipped with an ion pump and a titanium evaporation booster pump was installed and put into operation. As the CdS films prepared in the all-glass vacuum system at a pressure of 10^{-6} mm Hg gave better device characteristics than CdS evaporated in a bell jar system at 10^{-5} mm Hg, it seemed to be worthwhile to study CdS films prepared at lower pressures. Therefore, some effort was devoted to the installation and testing of the UHV system.

Furniture for the system was designed and built with three main objectives:

TABLE

AC Characteristics of Some Field Effect Triodes

Unit	Cadmium Sulfide Substrate Temp. (°C)	Operating Point V_D (Volt)	I_D (ma)	V_G (dc volt)	Transconductance g_m (Micromho)	Dynamic Drain Res. V_D (kΩ)	μ (Calculated) ($g_m \times V_D$)
113-2	100	7	5.7	15	500	3	1.5
99	175	18	3.0	15	125		
104-2	175	18	4.0	15	450	4	1.8
94-2	200	18	2.5	15	250	4	1
110-4	250	14	0.7	15	35	9	0.3
123-2	250	20	0.3	15	40	60	2
127-1	300	8	0.4	10	40	70	3

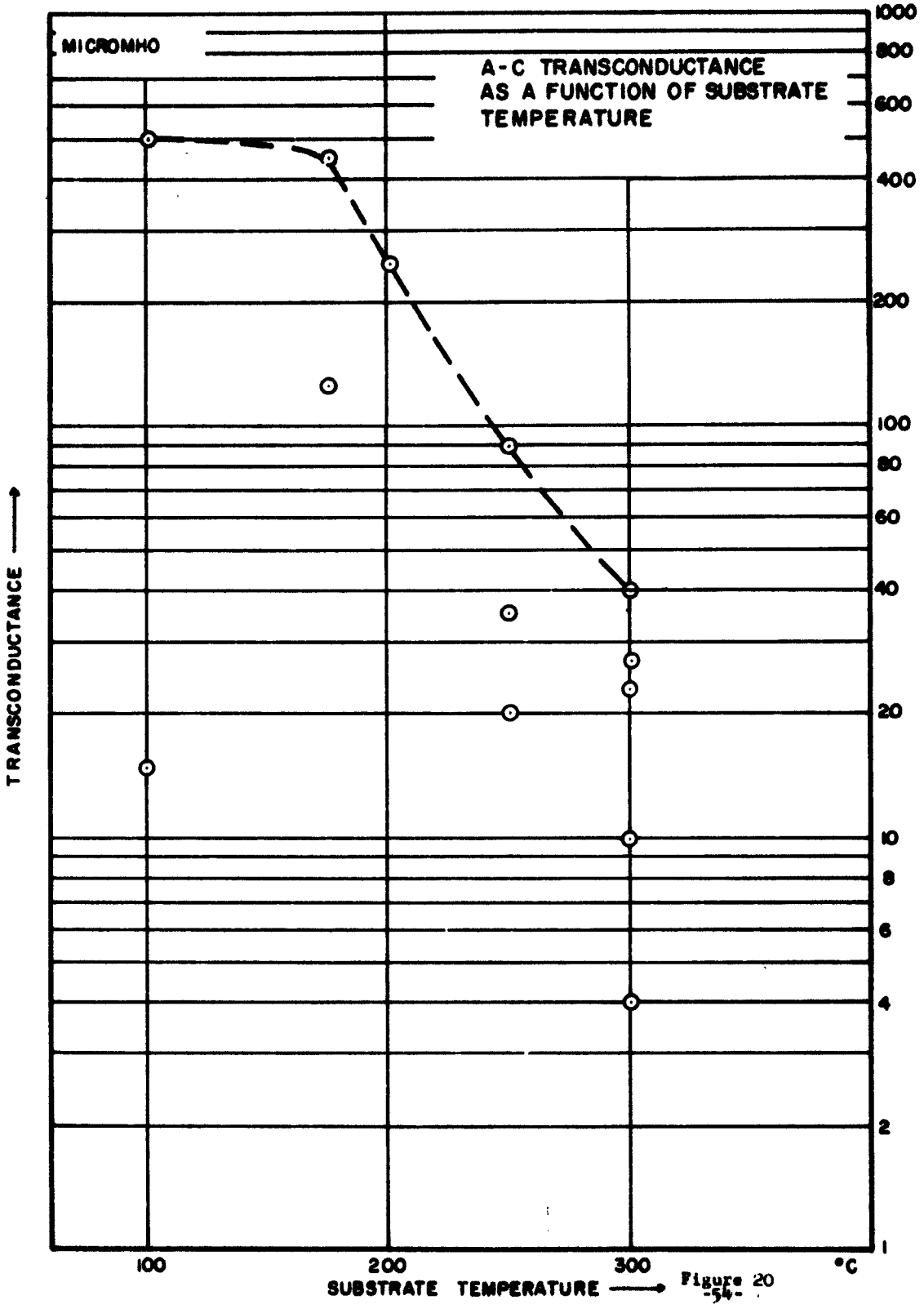
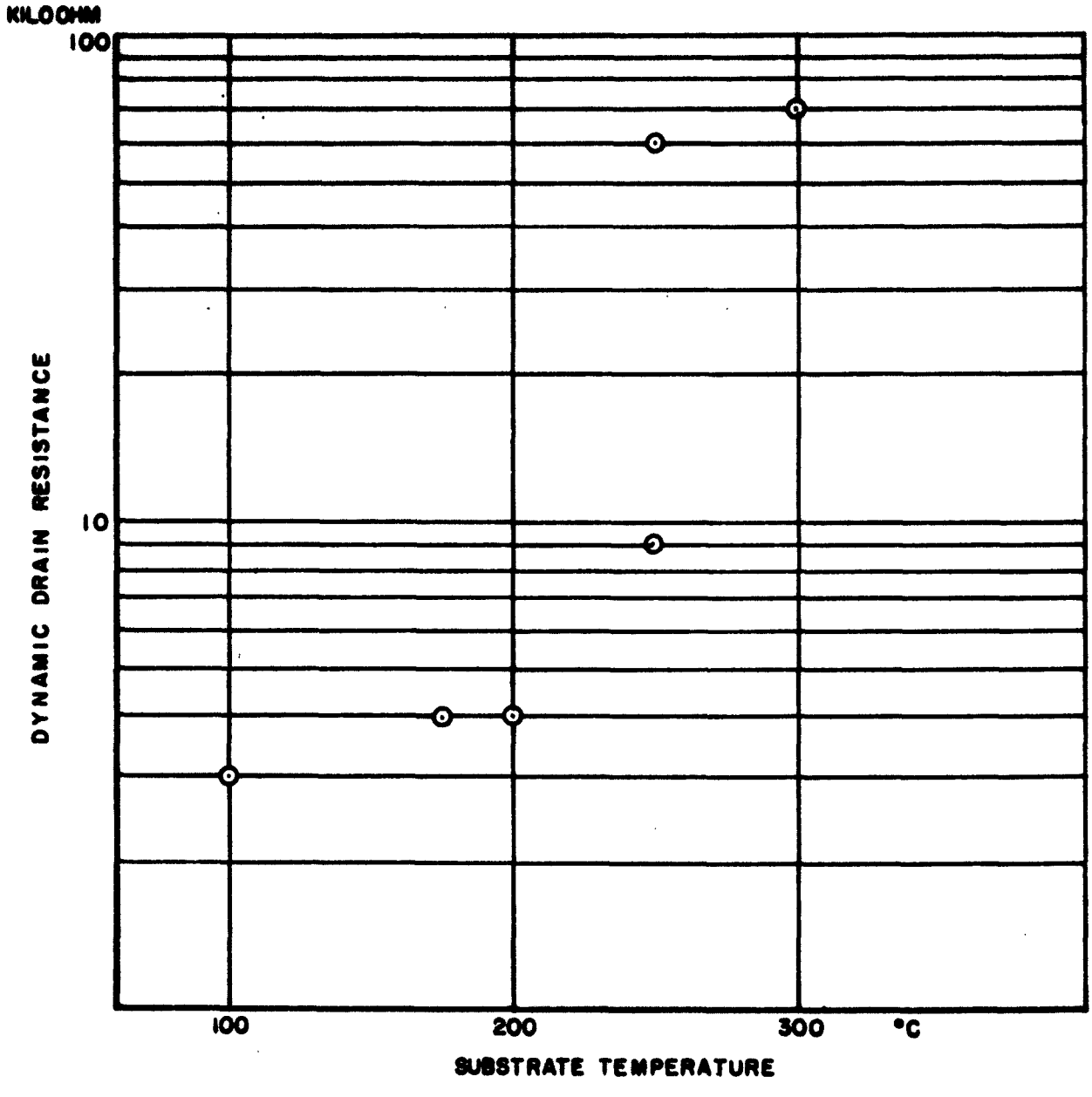

MICROMHO
A-C TRANSCONDUCTANCE
AS A FUNCTION OF SUBSTRATE
TEMPERATURE
1000
800
600
400
200
100
80
60
40
20
10
8
6
4
2
1
TRANSCONDUCTANCE
100
200
300
°C
SUBSTRATE TEMPERATURE

Figure 20



DYNAMIC DRAIN RESISTANCE AS A FUNCTION OF SUBSTRATE TEMP.

FIGURE 21

1. To avoid gas traps, like screws, which are difficult to pump out,

2. To reduce the contamination of the system during the evaporation by proper shielding, but

3. Without reducing the pumping speed significantly by reduced cross sections.

In order to bake the system, strip heaters were mounted around the ion pump and the bell jar. Without baking the system, silicon monoxide could be evaporated at 7×10^{-8} mm Hg. Cadmium sulfide could be evaporated only at about 6×10^{-7} mm Hg so far, but we expect to improve the vacuum by using a modified evaporation source and by baking the system.

4.8.3 Evaporation Sources

The form of the evaporation source has a significant influence on the characteristics of CdS films evaporated in a bell jar system. First an open crucible filled with CdS and heated from the top with a filament was used. Then a Drumheller source, which gave CdS film of higher resistivity and greater uniformity was used. A further improvement was achieved by using a source which approaches a molecular beam oven. The conditions for free molecular flow were first studied by M. Knudsen. A modern treatment of the problem is given by J. Dushman and I. Estermann.

The term molecular flow is used for a flow of molecules through an orifice or tube if the flow rate only depends on the area of opening and the diameter of the orifice is small compared to the mean free path of the molecules at the pressure of effusion. This condition can be realized for example by heating a material in a closed oven which only has a small opening. Molecular flow exists if the evaporation rate is much higher than the effusion rate and the mean free path of the molecules at the vapor pressure is smaller than the diameter of the orifice. The effusion rate F of an opening of area A in cm^2 in a very thin plate is given by

$$F = \frac{A\, v_a}{4} \qquad (cm^3\ sec^{-1})$$

if the average molecules velocity v_a of a molecule with molecular weight M at the temperature T°K is given in

$$v_a = 14{,}551\sqrt{\frac{T}{M}} \qquad (\text{cm sec}^{-1}).$$

It follows that the effusion rate is proportional to the reciprocal of the square root of the molecular weight. The evaporation of CdS from a molecular beam source, therefore, would start with a higher concentration of sulfur than cadmium in the beam. But this will change the composition of the gas phase in the oven until the rate of evaporation and effusion of both molecular species is the same. Starting from stoichiometric CdS the beam will have a stoichiometric composition after a short transient period.

An attempt will be made to improve our evaporation source to come closer to the ideal conditions for molecular beams.

Task IV: Zinc Oxide Material Improvement

4.9 Evaporation of Zinc Oxide

For all experiments "Baker Analyzed" Reagent Grade zinc oxide, a white powder was used. Zinc oxide has a melting point higher than 1800°C and sublimes at about the same temperature at normal pressure. No information about the vacuum deposition of zinc oxide could be found in the recent literature, although much work has been done on the electronic behavior of ZnO single crystals and some on sintered layers. Single crystals are usually prepared by a vapor phase reaction between zinc and oxygen at 1350°C.

Direct evaporation of zinc oxide in a vacuum system was attempted using several different evaporation sources. First a quartz crucible heated indirectly was used similar to that described in Section 4.5.1 of the previous report. At the high temperature which is necessary to evaporate ZnO the quartz crucible deteriorated, probably by forming a lower melting zinc silicate. The evaporation of ZnO from a ceramic crucible which was heated from the top by means of a tungsten spiral was more successful. A direct contact between ZnO and the tungsten wire should be avoided as coloration of the ZnO indicated a reaction between zinc oxide and tungsten at high temperatures. The use of a Drumheller source did not give an apparent advantage over the direct method.

The evaporation of the zinc oxide was rather irregular. There was no direct relation between the heater temperature and the evaporation rate. Apparently, decomposition of the zinc oxide took place, which may depend on the composition of the residual gas phase. The unheated parts of the vacuum system were covered with a dull gray coating which looked rather metallic. The same type of film was deposited on an unheated substrate. On heated substrates a smooth and transparent film was formed. A series of ZnO films deposited on pyrex glass slides at 3 different substrate temperatures showed the following resistivities.

Substrate Temperature	100°C	Resistivity 7×10^3 ohm-cm
	200°C	5×10^2
	300°C	7×10^2

The films were about 0.5 microns thick. Hall mobilities were not measurable. The noise in the Hall sample was rather high, in the order of 1 mV.

Since the resistivity of these films was in the same order of magnitude as the resistivity of CdS films in good field effect triodes, an attempt was made to incorporate these films into devices. The drain resistance at zero gate voltage was between 200 and 300 kilohm. None of the 6 samples constructed showed any activity. The samples behaved like simple resistor networks.

Substrate Temperature	100°C	Resistivity 7×10^3 ohm-cm
	200°C	5×10^2
	300°C	7×10^2

The films were about 0.5 microns thick. Hall mobilities were not measurable. The noise in the Hall sample was rather high, in the order of 1 mV.

Since the resistivity of these films was in the same order of magnitude as the resistivity of CdS films in good field effect triodes, an attempt was made to incorporate these films into devices. The drain resistance at zero gate voltage was between 200 and 300 kilohm. None of the 6 samples constructed showed any activity. The samples behaved like simple resistor networks.

V. CONCLUSIONS

The work during the past quarter has lead to the following conclusions.

TASK I: FIELD EFFECT TRIODES

(a) The conduction process in a CdS polycrystalline film exhibits an activation energy which can be altered by the electric field. The effect of the field on the activation energy is experimentally found to be approximately $-\Delta E \sim F^{\frac{1}{2}}$.

(b) It is necessary to introduce the concept of diffusion current of space charges in order to explain the experiments on class (2) triodes.

(d) If

(1) The source-CdS contact is assumed non-blocking (common and necessary assuption in all three mechanism models proposed), and

(2) the activation energy is assigned to distributive traps in CdS, THEN the trap emptying mechanism can explain the modulation of source-drain current by the gate voltage in both the class (1) and class (2) triodes (the difference between the two classes is then merely the source-drain RESISTANCE).

(e) The thickness of the insulating layer has a definite effect on device performance. Devices with thinner SiO layers exhibit much improved characteristics.

TASK II: SPACE CHARGE LIMITED TRIODES

(a) In order to improve the yield of working devices it has been decided to employ the field effect triode configuration of electrodes in the fabrication of space charge limited triodes.

(b) Cadmium sulfide films with resistivities up to 10^6 ohm centimeters can now be directly evaporated without subsequent atmosphere or heat treatment.

(c) The making of an ohmic contact to evaporated cadmium sulfide films is no longer a problem. Making good blocking layers is much more difficult.

TASK III: CADMIUM SULFIDE FILM IMPROVEMENT

(a) Post-deposition treatment of CdS films is capable of raising the resistivity by a factor of 10^4.

(b) Indium doping of the CdS film may significantly improve the properties.

(c) Evaporation of CdS in ultra-high vacuum should produce better device material.

TASK IV: ZINC OXIDE MATERIAL IMPROVEMENT

(a) The evaporation of zinc oxide in vacuum is difficult to control.

(b) Field effect devices in which cadmium sulfide was replaced by zinc oxide did not show any activity.

VI. PROGRAM FOR NEXT INTERVAL

TASK I: FIELD EFFECT TRIODES

Further measurements of the type described in section 4.1.3 will be carried out to verify the theoretical model proposed.

The study of cadmium sulfide film thickness on device performance will be continued to find optimum thickness for various substrate temperatures used.

New evaporation sources for cadmium sulfide will be studied.

TASK II: SPACE CHARGE LIMITED TRIODES

Two terminal devices will be fabricated to study the effect of electrodes and the evaporation parametem of CdS films on space charge limited currents. An attempt will be made to derive trap properties from the temperature dependence of space charge limited currents.

The fabrication of space charge limited triodes will be postponed until more basic information on space charge limited currents in evaporated films is obtained.

TASK III: CADMIUM SULFIDE FILM IMPROVEMENT

The possibility of controlling the resistivity of a CdS film with some precision by a post-deposition treatment in a hydrogen-hydrogen sulfide mixture calculated to maintain a 1:1 ratio of Cd:S at the temperature of the treatment in the gas phase (or any other ratio found to be desirable) will be investigated. The gas mixture would be saturated with CdS from a powder source before reaching the sample.

The effect of In doping of the sample will be studied by placing In in the gas stream ahead of the sample under treatment. A systematic study of differences in the properties of CdS films prepared in a normal vacuum system and in the ultra high vacuum system will be carried out.

TASK IV: ZINC OXIDE MATERIAL IMPROVEMENT

Zinc oxide films will be deposited by sputtering. Sputtered zinc oxide films will be incorporated in field effect devices.

VII. IDENTIFICATION OF PERSONNEL

A. Biographical Data

Dr. John M. Blank

Dr. Blank received his AB in Physics from the College of Wooster in 1947, and his MS and PhD in Physics from MIT in 1950 and 1952 respectively. From 1948 to 1952, he was a Research Assistant with MIT's Project Whirlwind. During this period he was concerned with the design and development of electrostatic storage tubes for computer memory units, and pilot plant production of these tubes.

In 1952, he joined the Electronics Laboratory. Since that time he has been involved in the development of ferrite and dielectric ceramic materials, phase equilibria of magnetic materials, oxygen ferrite equilibrium relationships, the development of TV components and memory cores on a pilot plant reduction scale.

For the past two years he has had the responsibility for various projects concerning all phases of thin circuit microelectronic fabrication and study. He has directed all of the initial materials and processes effort of the Electronics Laboratory in the field of thin film microelectronics, and continues to be responsible for a majority of the new developments in the materials and processes field. He has been instrumental in developing a large share of the Company's passive component technology as well as their efforts in the field of thin film active devices. Under his direction, the thin film diode development program has achieved considerable success, and during the past year he has directed the Laboratory's research and development efforts on thin film active devices.

Dr. W. Tantraporn

Dr. Tantraporn received his B.S. from the University of Denver in 1952, and his M.S. and Ph.D. degrees in Physics from the University of Michigan in 1953 and 1958 respectively. Prior to joining the General Electric Company's Electronics Laboratory in 1959, he was a lecturer in physics at the University of Michigan.

At the Electronics Laboratory he has been actively engaged in both the theoretical and experimental aspects of microelectronic research and development. In this regard, he has done extensive work in the fields of tunneling, Schottky emission, dielectric breakdown, and polymerization. He has been instrumental in clearing up the considerable controversy that exists with regard to the mechanism of emission in thin film active devices. His experiments on the determination of the apparent penetration of electrons through thin metallic films represent a significant contribution to this field, and in effect have removed the most serious obstacle to the completion of a thin film "hot electron" triode. He was the first to show that the current-voltage relationship for injection of electrons over a potential barrier in typical thin film active devices followed a thermionic rather than a tunneling mechanism at ordinary temperatures.

Dr. K.K. Reinhartz

Dr. Reinhartz received his diploma Chemiker and Ph.D. degrees in Physical Chemistry from the Technische Hochschule, Hanover, Germany, in 1956 and 1959 respectively. His doctoral dissertation was on the subject of phase equilibria in hydrogen-hydrocarbon systems at high pressures and temperatures.

In 1959 Dr. Reinhartz joined the "German Nuclear Research Center" at Karlsruhe, Germany, where he was engaged in research in the use of -emitting radionuclides in self-luminous materials. He was involved in a research effort in reprocessing of irradiated nuclear fuels in an integrated fuel cycle for a fast breeder reactor.

Since joining the Solid State Materials group in October 1961, Dr. Reinhartz has been engaged in the development of thin film active devices. His most recent work has been concerned with the deposition of cadmium sulfide and construction of space charge limited thin film devices.

Mr. Warren L. Willis

Mr. Willis received a B.S. in Engineering Physics in 1960 from Kansas University. He graduated with highest honors.

He joined the General Electric Company in June, 1960, as a member of Electron Devices where he worked in the field of thermoelectricity, primarily on the encapsulation of materials. Since October, 1960, he has been a member of the Solid State Materials group, where he has continued his work in thermoelectricity, metal to ceramic eutectic bonding and other solid state studies. More recently, Mr. Willis has been involved in the development of electrode structures for field effect triodes.

Mr. Willis is a member of Tau Beta Pi and Sigma Pi Sigma.

Dr. A.E. Cahill

Dr. Cahill received his B.S. degree in Chemistry from the University of Chicago in 1948. In 1951 he was awarded the Ph.D. from Chicago in Physical Chemistry for his study "The Use of Heavy Oxygen in the Study of Reactions of Hydrogen Peroxides".

In 1951 he joined the Electronics Laboratory of the General Electric Company. Much of his work since then has been in the field of Electrochemistry. He has done work on the chemical deposition and metal films; i.e., development of "electroless" copper and silver; and fractionation of stabilized isotopes in homogeneous reactions.

He transferred to the Solid State Materials group in 1961 where he has worked on fuel cells, and lately in microelectronics. In the latter field he has been involved in the glow discharge method of depositing dielectric films; such as, TiO_2 and $PbTiO_3$ for capacitor dielectrics.

Recently, Dr. Cahill has been involved in the program investigating the effect of hydrogen sulfide-hydrogen atmospheres on cadmium sulfide films. This program is designed to explore ways of changing the electrical characteristics of cadmium sulfide films after deposition. It also is possible to actually move cadmium sulfide from one place and deposit it in another at relatively high pressures by this method. The feasibility of this procedure for actual deposition of films is also being investigated.

Dr. Cahill is the holder of a patent on Chemically Deposited Copper, and is the author of several papers on physical chemistry.

Dr. Virginia A. Russell

Dr. Russell received her B.S. in Chemistry from Westminister College in 1947, and her M.S. and Ph.D. from Syracuse University in 1949 and 1953 respectively. Her doctoral dissertation was entitled "Crystal Structure of Ammonium Sulfamate". From 1947 to 1952 she taught undergraduate courses at Syracuse University and from 1952-1955 she was a University Research Associate. During this period she was concerned with the preparation and analysis of magnesium-boron compounds, and the determination of the structure of these compounds and their decomposition products utilizing X-ray methods.

In 1955 she joined the Solid State Materials group of the Electronics Laboratory as a Physical Chemist. Since then, she has performed most of the X-ray investigations performed in the laboratory. She has also been concerned with the development of high temperature resistors, high density and high dielectric strength barium strontium titanates, thermoelectricity, and has coordinated various aspects of the Laboratory's Microelectronics program. Most recently she has developed methods for the preparation of single crystal platelets of silicon on glass substrates and single crystals of cadmium sulfide.

B. Approximate Engineering Man Hours (1 Dec 1962 - 28 Feb 1963)

J.M. Blank	31 Hours
W. Tantraporn	131
K.K. Reinhartz	144
V.A. Russell	*
A.E. Cahill	*
W.L. Willis	344
Total	650

*These personnel carried out work on a closely related company-sponsored program and their work is reported in this document.

VIII. REFERENCES

1. P.K. Weimer, Proc. IRE 50, 1462, (1962).
2. H.K.J. Ihantola, Tech. Rep. No. 1661-1, Aug. 17, 1961, Solid State Electronics Lab., Stanford University.
3. Melpar, Inc., Eleventh Quarterly Report on "Molecular Circuit Development," submitted to U.S. Dept. of the Navy, Bu. Weapons, Washington 25, D.C. (Contract No. NOw 60-0362-c, 1963).
4. W. Tantraporn and K.K. Reinhartz, Proc. of NEC 18, 736, (1962).
5. R. Zuleeg, an unpublished report (Hughes Aircraft Co., Semiconductor Div., Newport Beach, California.
6. G.T. Wright, J. of Brit. IRE, 20, 337, 1960.
7. General Electric Co., Second Quarterly Report on Field Effect Triodes and Space Charge Limited Triodes, submitted to USARDL, Fort Monmouth, New Jersey (SC Contract No. DA-36-039-sc-90756, 1962-3).
8. H. Borkan and P.K. Weimer, NEREM Record IV, Lewis Winner, New York, 158, (1962).
9. P.R. Emtage and W. Tantraporn, Phys. Rev. Letters 8, 267, (1962).
10. J.C. Maxwell, A Treatise on Electricity and Magnetism, Vol I, 3rd Ed., Oxford Univ. Press, London (1892), article 202. (Reprints by Lowe and Brydone Printers, Ltd., London (1946), p. 309.).
11. W.W. Piper and R.E. Halsted, "Intrinsic Electrical Properties of n-type CdS," Proceedings of the International Conference on Semiconductor Physics, Prague 1960, Publishing House of Czech. Academy of Sciences, Prague.

VIII. REFERENCES

1. P.K. Weimer, Proc. IRE 50, 1462, (1962).
2. H.K.J. Ihantola, Tech. Rep. No. 1661-1, Aug. 17, 1961, Solid State Electronics Lab., Stanford University.
3. Melpar, Inc., Eleventh Quarterly Report on "Molecular Circuit Development," submitted to U.S. Dept. of the Navy, Bu. Weapons, Washington 25, D.C. (Contract No. NOw 60-0362-c, 1963).
4. W. Tantraporn and K.K. Reinhartz, Proc. of NEC 18, 736, (1962).
5. R. Zuleeg, an unpublished report (Hughes Aircraft Co., Semiconductor Div., Newport Beach, California.
6. G.T. Wright, J. of Brit. IRE, 20, 337, 1960.
7. General Electric Co., Second Quarterly Report on Field Effect Triodes and Space Charge Limited Triodes, submitted to USARDL, Fort Monmouth, New Jersey (SC Contract No. DA-36-039-sc-90756, 1962-3).
8. H. Borkan and P.K. Weimer, NEREM Record IV, Lewis Winner, New York, 158, (1962).
9. P.R. Emtage and W. Tantraporn, Phys. Rev. Letters 8, 267, (1962).
10. J.C. Maxwell, A Treatise on Electricity and Magnetism, Vol I, 3rd Ed., Oxford Univ. Press, London (1892), article 202. (Reprints by Lowe and Brydone Printers, Ltd., London (1946), p. 309.).
11. W.W. Piper and R.E. Halsted, "Intrinsic Electrical Properties of n-type CdS," Proceedings of the International Conference on Semiconductor Physics, Prague 1960, Publishing House of Czech. Academy of Sciences, Prague.

Distribution List

	Number of Copies
OASD (R and E), Rm 3E1065 Attn: Technical Library the Pentagon Washington 25, D. C.	1
Chief of Research and Development OCS, Department of the Army Washington 25, D. C.	1
Commanding Officer US Army Electronics Command Attn: AMSEL-AD Fort Monmouth, New Jersey	1
Director US Naval Research Laboratory Attn: Code 2027 Washington 25, D. C.	1
Commanding Officer and Director US Navy Electronics Laboratory San Diego 52, California	1
Commander Aeroanutical Systems Division Attn: ASAPRL Wright-Patterson Air Force Base, Ohio	1
Commander Air Force Cambridge Research Laboratories Attn: CRXL-R L G Hanscom Field Bedford, Massachusetts	1
Commander Air Force Command and Control Development Division Attn: CRZC L G Hanscom Field Bedford, Massachusetts	1
Commander Rome Air Development Center Attn: RAALD Griffiss Air Force Base, New York	1

DA 36-039-sc-90756
General Electric Company

3rd Quarterly Report
1 Dec 62 - 28 Feb 63

Distribution List

	Number of Copies
OASD (R and E), Rm 3E1065 Attn: Technical Library the Pentagon Washington 25, D. C.	1
Chief of Research and Development OCS, Department of the Army Washington 25, D. C.	1
Commanding Officer US Army Electronics Command Attn: AMSEL-AD Fort Monmouth, New Jersey	1
Director US Naval Research Laboratory Attn: Code 2027 Washington 25, D. C.	1
Commanding Officer and Director US Navy Electronics Laboratory San Diego 52, California	1
Commander Aeroanutical Systems Division Attn: ASAPRL Wright-Patterson Air Force Base, Ohio	1
Commander Air Force Cambridge Research Laboratories Attn: CRXL-R L G Hanscom Field Bedford, Massachusetts	1
Commander Air Force Command and Control Development Division Attn: CRZC L G Hanscom Field Bedford, Massachusetts	1
Commander Rome Air Development Center Attn: RAALD Griffiss Air Force Base, New York	1

DA 36-039-sc-90756 **Number of Copies**

Commanding General
US Army Material Command
Attn: R and D Directorate
Washington 25, D. C. 1

Commanding Officer
US Army Communications and Electronics Combat Development Agency
Fort Huachuca, Arizona 1

Commander
Armed Services Technical Information Agency
Attn: TISIA
Arlington Hall Station
Arlington 12, Virginia 10

Chief
US Army Security Agency Board
Arlington Hall Station
Arlington 12, Virginia 2

Deputy President
US Army Security Agency Board
Arlington Hall Station
Arlington 12, Virginia 1

Commanding Officer
Harry Diamond Laboratories
Attn: Library, Rm. 211, Bldg. 92
Washington 25, D. C. 1

Commanding Officer
US Army Electronics Material Support Agency
Attn: SELMS-ADJ
Fort Monmouth, New Jersey 1

Corps of Engineers Liaison Office
US Army Electronics R and D Laboratory
Fort Monmouth, New Jersey 1

AFSC Scientific/Technical Liaison Office
US Naval Air Development Center
Johnsville, Pennsylvania 1

Advisory Group on Electron Devices
346 Broadway
New York 13, New York 2

DA 36-039-sc-90756

	Number of Copies
Marine Corps Liaison Office US Army Electronics R and D Laboratory Fort Monmouth, New Jersey	1
Commanding General US Army Combat Developments Command Attn: CDCMR-E Fort Belvoir, Virginia	1
Headquarters Electronic Systems Division Attn: ESAT L G Hanscom Field Bedford, Massachusetts	1
Commanding Officer US Army Electronics Research Unit P.O. Box 205 Mountain View, California	1
Commanding Officer Attn: ORDES-FEL Frankford Arsenal Philadelphia 37, Pennsylvania	1
Commanding Officer Attn: OMRO Watertown Arsenal Watertown, Massachusetts	1
Commanding General Attn: Technical Library Redstone Arsenal Huntsville, Alabama	1
Bell Telephone Labs Attn: R. Ryder Murray Hill, New Jersey	1
Motorola, Inc. Microelectronics Laboratory Attn: JR Black, Mgr. 3102 N 56th Street Phoenix, Arizona	1
Philco Research Laboratory Attn: Mr. James Spratt Blue Bell, Pennsylvania	1

DA 36-039-sc-90756

	Number of Copies
Electro-Optical Systems, Inc. Attn: Dr. I. Wieman 125 North Vinedo Avenue Pasadena, California	1
General Precision, Inc. Attn: Dr. H.M. Pallack Kearfott Division Clifton, New Jersey	1
Mr. B.M. Buckingham Johns Hopkins Applied Physics Laboratory 8621 Georgia Avenue Silver Spring, Maryland	1
Parma Research Laboratory Attn: Dr. R.G. Breckeridge Union Carbide Corporation Parma, Ohio	1
International Resistance Co. Attn: Dr. S. Hirshon 401 Broad Street Philadelphia, Pennsylvania	1
Radio Corporation of America Attn: Dr. H. Johnson Princeton, New Jersey	1
A.D. Little Company Attn: Dr. G. Rudenberg Cambridge, Massachusetts	1
Melpar, Inc. Attn: Dr. C. Feldman 3000 Arlington Blvd. Falls Church, Virginia	1
Autonetics Attn: Dr. Arnold Miller 3400 E. Anoheim Road Anaheim, California	1
Director Fort Monmouth Office US Army Communications and Electronics Combat Development Agency Fort Monmouth, New Jersey	1

DA 36-039-sc-90756 **Number of Copies**

Mr. A.H. Young Code 618AIA Semiconductor Group Bureau of Ships Department of the Navy Washington 25, D.C.	1
Commanding Officer US Army Electronics R and D Laboratory Fort Monmouth, New Jersey	
Attn: Director of Research/Engineering	1
Attn: Ch, Technical Documents Center	1
Attn: Ch, Technical Information Division	3
Attn: Rpts Dist Unit, Solid State and Frequency Cont Div (record cy)	1
Attn: Ch, M and QE Br., Solid State and Frequency Cont Division	1
Attn: Director, Solid State and Frequency Cont Division	1
Attn: W. Glendinning, Solid State and Frequency Cont Div.	1
Total number of copies to be distributed	60

AD

General Electric Co., Electronics Laboratory, Syracuse, N.Y. FIELD EFFECT TRIODES AND SPACE CHARGE LIMITED TRIODES by JH Blank, AE Cahill, KK Reinhartz, VA Russell, W Tantraporn, and WL Willis. Third Quarterly Progress Report, 1 December 1962-28 February 1963. 71 p. incl. line drawings and photographs. (Contract DA 36-039-sc-90756)

Unclassified Report

The purpose of this project is the theoretical investigation, design, and development of thin film metal-dielectric active solid state devices with usable power gains that are relatively insensitive to temperature changes.

A detailed conduction mechanism for thin-film field effect triodes is presented. The results of experiments in varying SiO and CdS thickness in field effect triodes are shown. Effects of device aging and electrode configurations on device performance are also discussed.

The requirements for producing space charge limited current in devices and possible methods of fulfilling them are discussed. Experimental results in fabricating devices using different source and drain electrode materials are shown.

A post-deposition treatment of cadmium sulfide films is outlined and results are presented. Preparation of CdS films at various substrate temperatures and in ultra-high vacuum is discussed. The use of molecular beam evaporation sources is also discussed.

UNCLASSIFIED

1. Thin Films
2. Cadmium Sulfide Coatings
3. Thin Film Active Devices

I. Blank, JH
II. Cahill, AE
III. Reinhartz, KK
IV. Russell, VA
V. Tantraporn, W
VI. Willis, WL
VII. Contract No. DA-36-039-sc-90756

UNCLASSIFIED

AD

General Electric Co., Electronics Laboratory, Syracuse, N.Y. FIELD EFFECT TRIODES AND SPACE CHARGE LIMITED TRIODES by JH Blank, AE Cahill, KK Reinhartz, VA Russell, W Tantraporn, and WL Willis. Third Quarterly Progress Report, 1 December 1962-28 February 1963. 71 p. incl. line drawings and photographs. (Contract DA 36-039-sc-90756)

Unclassified Report

The purpose of this project is the theoretical investigation, design, and development of thin film metal-dielectric active solid state devices with usable power gains that are relatively insensitive to temperature changes.

A detailed conduction mechanism for thin-film field effect triodes is presented. The results of experiments in varying SiO and CdS thickness in field effect triodes are shown. Effects of device aging and electrode configurations on device performance are also discussed.

The requirements for producing space charge limited current in devices and possible methods of fulfilling them are discussed. Experimental results in fabricating devices using different source and drain electrode materials are shown.

A post-deposition treatment of cadmium sulfide films is outlined and results are presented. Preparation of CdS films at various substrate temperatures and in ultra-high vacuum is discussed. The use of molecular beam evaporation sources is also discussed.

UNCLASSIFIED

1. Thin Films
2. Cadmium Sulfide Coatings
3. Thin Film Active Devices

I. Blank, JH
II. Cahill, AE
III. Reinhartz, KK
IV. Russell, VA
V. Tantraporn, W
VI. Willis, WL
VII. Contract No. DA-36-039-sc-90756

UNCLASSIFIED